Abstract—Design methodologies for Hitachi's RISC microprocessors and microcontrollers are discussed. One of the processors is a high-end PA-RISC™. The others, the PA/50 and the SH series microcontroller, are low power and low cost processors. Low cost processors require small chip size and short design time. To shorten the architecture level design time, we have developed a RT-level behavior simulation tool based on C language. And to reduce the total design time, we use a gate-level synthesis program from the behavior model description. This approach resulted in the low power 42 MIPS/W PA-RISC™ processor (the PA/50, which run at a 33 MHz clock rate) being completed within 15months. Another approach to minimizing chip size while maintaining high performance is to reduce the design turnaround time by using microcode instead of direct wired logic design. We wrote 480-word microcodes equivalent to a 5.8K transistor logic. After assigning the control stages for the microcode fields, we used an in-house logic synthesis and optimized for performance and chip size. The CPU core of the SH series microcontroller occupies only 8 mm² including CPU core and multiplier circuit. The processor reaches 16 MIPS at 20 MHz. It took 17 man-months to realize a minimum 8 mm² chip. The total control logic consists of 27 thousand transistors.

I. Hitachi RISC processors

We have developed variety of processor chips. One is a high-end superscalar PA-RISC™ processor chip, running at a 120-MHz clock rate. This processor integrates 2.8 million transistors within a chip area 16.2 mm by 16.5 mm. The other chips are a low-cost PA-RISC™ processor for an entry model workstation engine and a Hitachi original RISC, the SH series microcontroller for embedded and multimedia applications. The low-cost PA-RISC™ processor, the PA/50, is characterized by low power consumption. It implements a power save mode. Software control can reduce its clock frequency to one eighth of the peak rate. On-chip memories, caches and TLBs, have been the major consumers in percentage, so we used a DRAM-type low-power sense amplifier for the memories. The PA/50 is fully compatible with the PA-RISC™ architecture. Another design goal of the PA/50 was a low system cost. To meet this goal, we designed the chip to provide high performance without using external cache memories. To get a high hit ratio in the on-chip caches, we chose two-way set-associative data and instruction caches instead of direct mapped cache memories. The sizes of the data and instruction caches are respectively 4 Kbytes and 8 Kbytes. A non-blocking cache is implemented to reduce the miss penalty. Block TLBs are also implemented, and the memory interface is tailored for synchronous DRAM. The PA/50 achieves 55 VAX MIPS and under normal program conditions consumes only 1.3 watts at 33 MHz. This low power consumption allows it to be packaged in 160-pin plastic QFP.

For embedded and multimedia applications, the SH series provides low power consumption, low system cost, high system performance, and high integration embodying DSP functions as well as on-chip peripherals. The instruction set is optimized for the code density, and all instructions are 16 bits long. To minimize the chip size while maintaining high system performance, we used a wired logic approach for the control circuits. A DSP function is implemented by combining an arithmetic unit in the CPU and an independent multiplier circuit. The CPU and multiplier respectively contain 39 thousand and 9.5 thousand transistors. The clock cycle is 20 MHz at a 5-volt power supply and 12.5 MHz at 3.3 V. Photograph shows a microphotograph of a second generation SH system with a large peripheral mix including 4 K-byte cache memory Bus control circuits. The chip size is a 9.5 mm by 8.7 mm with a 450 thousand transistors.

II. Design methodologies in Hitachi

Each processor has specific requirements, and for the high-end processor, the predominant one is precise delay management. We used our proprietary placement and routing program running on our main-frame computer, and we used a supercomputer-based high-speed-logic simulation program. Two low-power and low-cost processors aim for entry model workstation engine and embedded controller. Because small chips and short design times are especially important for low-cost processors. In designing the PA/50, we have emphasized the short design time. We de-
veloped an RT-level behavior simulation tool based on C language so that bugs could be removed as early as possible. Simulation speed is also important in reducing the design time and the behavior level simulation ran at 200 to 1200 cycles per second on a 60-MIPS workstation. Seventy-four thousand RT-level C steps were needed to simulate a processor with 1.28 million transistors. For debugging and control purposes, we needed additional 58 thousand C steps. One tenth of the 1.28 million transistors are for the random logics, and to reduce the total design time, we further applied a gate level logic synthesis directly from the behavior model as much as possible. To utilize the Synopsis logic synthesis program, we developed an in-house translator for converting from the RT-level model to truth tables. After the synthesis, we used workstation-based layout tools. This approach resulted in the low power 42MIPS/W PA-RISC™ processor, which is runs at a 33-MHz clock rate, being completed within 15 months.

We took a new chip size minimizing approach maintaining a short design time and high performance for the SH series microcontroller. The approach is characterized by the logic design it uses to generate wired logic gates from micro-code descriptions. To provide single-cycle execution at a high clock rate, we have chosen a wired logic approach like that in RISC processors. Wired logic, however, result in a long design time because of its design complexity. Our design goal for the SH series was to reduce the design turn-around time by using microcode instead of direct random gate design. We wrote 480-word microcodes for a logic with 5.8 thousand transistors and the total control logic was 27 thousand transistors. For the PA/50, one C step represented 16 transistors, including caches and TLBs. As far as the random logic portion is concerned, it is 3.8 transistors. For the microcode design of SH microcontroller, one microcode represents 12 transistors. We think the microcode approach is an alternative solution to random logic design. After assigning the control codes of the state diagram to the microcode fields, we used an in-house logic synthesis program and optimized for performance and chip size. The logic synthesis deals not only with gate generation but also with size minimizing. Final block and inter-block layout were done on a main-frame computer. The CPU core of our microcontroller occupies only 8 mm² including CPU core and multiplier circuit. This microcontroller reaches 16 MIPS at a 20-MHz clock rate and it required 17 man-months to design and build a 8 mm² chip.