Session 28: Design Representations and Data Structures for High Level Design

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The problems of representing a design and storing the information in an efficient and meaningful way are central to the design process. The papers in this session discuss approaches to these problems by using novel incremental methods, by proposing reducing redundancies in VHDL, and by creating a BDD data structure for formal design verification.

28.1 A SYSTEM FOR INCREMENTAL SYNTHESIS TO GATE-LEVEL AND REOPTIMIZATION FOLLOWING RTL DESIGN CHANGES
Share C. Prasad, P. Anirudhan, Patrick W. Bosshart

28.2 LESSONS IN LANGUAGE DESIGN: COST/BENEFIT ANALYSIS OF VHDL FEATURES
Oz Levia, Serge Maginot, Jacques Rouillard

28.3 HSIS: A BDD-BASED ENVIRONMENT FOR FORMAL VERIFICATION