Session 21A: Formal Verification

Chair: Ron Collett

When we use the term "formal verification" in system design, we generally mean using methods of mathematical proof rather than simulation and testing to insure the quality of a design. Numerous benefits are claimed for the formal verification approach over simulation. The primary benefit is that formal verification covers all possible behaviors of a model, whereas simulation can miss important behaviors. Thus, formal verification can improve the robustness of a design. Development time can also be reduced using formal methods since bugs are caught in earlier stages of the design process.

In this presentation, we will consider the various stages of the design process, and how the tools and methods of formal verification fit into these design stages. The emphasis will be on methods that appear to have the most promise for practical application in the near future.

21A.1 FITTING FORMAL METHODS INTO THE DESIGN CYCLE

Ken McMillan