Session 20: FPGA Placement and Routing

**Chair:** Dwight D. Hill

Field programmable technology provides many challenges to successful routing. The set of routing resources is limited and largely preconfigured. These papers explore ways to turn these problems into virtues, resulting in higher completion rates and performance.

**20.1 PLACEMENT AND ROUTING FOR A FIELD PROGRAMMABLE MULTI-CHIP MODULE**
Sanko H. Lan, Avi Ziv, Abbas El Gamal

**20.2 PERFORMANCE-DRIVEN SIMULTANEOUS PLACE AND ROUTE FOR ROW-BASED FPGAS**
Sudip K. Nag, Rob A. Rutenbar

**20.3 LAYOUT DRIVEN LOGIC SYNTHESIS FOR FPGAS**
Shih-Chieh Chang, Kwang-Ting Cheng, Nam-Sung Woo, M. Marek-Sadowska