FPGAs have become an important means of quickly implementing digital systems. Because of their special structure and limited size they require special partitioning techniques. This session presents new results for this problem and a clock skew minimization solution.

16.1 CLOCK SKEW MINIMIZATION DURING FPGA PLACEMENT
Kai Zhu, D.F. Wong

16.2 MULTI-WAY NETLIST PARTITIONING INTO HETEROGENEOUS FPGAS AND MINIMIZATION OF TOTAL DEVICE COST AND INTERCONNECT
Roman Kuznar, Franc Brgiez, Baldomir Zajc

16.3 CIRCUIT PARTITIONING FOR HUGE LOGIC EMULATION SYSTEMS
Nan-Chi Chou, Lung-Tien Liu, Chung-Kuan Cheng, Wei-Jin Dai, Rodney Lindelof