Session 12: Technology-Driven Routing

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In Field Programmable Gate Array technologies, routability and interconnect delays depend on the choice of the upper bounds or the number of programmable switches used in routing. The first paper presents algorithms for determining such upper bounds for all nets simultaneously such that performance constraints are fulfilled. The second paper proposes routing algorithms for a new FPGA architecture. The third paper describes a global routing method which uses bipolar specific features to improve performance. The fourth paper addresses four-layer routing which allows arbitrary terminal locations.

12.1 SWITCH BOUND ALLOCATION FOR MAXIMIZING ROUTABILITY IN TIMING-DRIVEN ROUTING OF FPGAS
Kai Zhu, D.F. Wong

12.2 ROUTING IN A NEW 2-DIMENSIONAL FPGA/FPIC ROUTING ARCHITECTURE
Yachyang Sun, C.L. Liu

12.3 A GLOBAL ROUTER OPTIMIZING TIMING AND AREA FOR HIGH-SPEED BIPOLAR LSI'S
Ikuo Harada, Hitoshi Kitazawa

12.4 A UNIFIED APPROACH TO MULTILAYER OVER-THE-CELL ROUTING
S. Madhwapathi, Naveed A. Sherwani, Siddharth Bhingarde, Anand Panyam