Session 10: Estimation and Synthesis of Memory Structures
Chair: Gaetano Borriello

Storage elements account for a large fraction of the area in ASICs for regular computations. The three papers in this session address the synthesis of storage elements in DSP, scientific, and iterative algorithms.

10.1 MEMORY ESTIMATION FOR HIGH LEVEL SYNTHESIS
Ingrid Verbauwhede, Chris Scheers, Jan Rabaey

10.2 MINIMIZATION OF MEMORY TRAFFIC IN HIGH-LEVEL SYNTHESIS
David J. Kolson, Alexandru Nicolau, Nikil Dutt

10.3 SEQUENCER-BASED DATA PATH SYNTHESIS OF REGULAR ITERATIVE ALGORITHMS
Mohammed Aloqeely, C.Y. Roger Chen