A Slew-Rate Controlled Output Driver with One-Cycle Tuning Time

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Abstract

A low-power slew-rate controlled output driver with open loop digital scheme, one-cycle lock time is presented. Proposed output driver maintains slew rate in the range of 2.1V/ns to 3.6V/ns in a one cycle after the enable clock is inserted. It is implemented in 0.18um CMOS process, and the control block consumes 13.7mW at 1Gbps.

Introduction

Memory and storage device interface speeds have increased from several hundred Mbps to a couple of Gbps in recent times. Consequently, the increased data rate and signal frequency has given rise to several effects, specifically the large current produced by several CMOS output drivers generates noise on the inductive bond wire and package and board traces. Moreover, inadequate termination, cross-talk and transmission line timing problem are other serious sources of power noise. The slew-rate controlled output drivers are able to minimize the power noise without degradation in performance. Shin et al. proposed slew rate controlled output driver using PLL in which replica of VCO delay cell is used as an output driver [1]. After the PLL is locked, VCO bias voltages are generated and they feed the slew-rate control block to produce appropriate control signals which are utilized to control the slew-rate of the output driver. However, PLL is a high order system and consumes large area and power. Moreover, it takes a long time to lock the system. For use in 1Gbps 512-Mb DDRII SDRAM, the slew-rate controlled output driver is proposed by Matano et al. [2]. This output driver is composed of a base driver, PMOS and NMOS impedance-control circuits, and a slew-rate control circuit. The slew-rate control signals are generated during the impedance-adjust mode and the drive mode. This method takes tens of cycles to generate the slew-rate control signals. An output driver using speed-locked-loop (SLL) in PCI application was proposed recently [3]. In it, digitally controlled oscillator (DCO) is used to detect the PVT variations with the speed constant to produce control signals named the speed bus. Slew-rate of the output driver is then controlled by the 3-b speed bus. The output driver is a replica of a DCO delay cell. SLL has advantages over conventional circuits in terms of locking time, stability, and power consumption. However, it still takes eight cycles for correct locking due to the feedback part of SLL.

In present work, an open-loop slew-rate controlled output driver with one-cycle lock time is proposed. By utilizing all digital open-loop architecture, this output driver occupies small area and can keep the slew rate constant even with various PVT changes with one-cycle lock time, which enables output-on-demand and reduces standby current while updating the control signal promptly.

Architecture

Block diagram of the proposed slew-rate controlled output driver is shown in Fig. 1. The proposed circuit is composed of three units: PVT variation detector, select signal generator, and segmented output driver. The PVT variation detector detects process, voltage, and temperature variations. The select signal generator generates control signals using input from the PVT variation detector in order to decide the drive strength of the output driver. The last block is a segmented output driver that sends the input data signal to the output with a constant slew-rate.

Circuits and Operations

Fig. 2 shows the schematic and fundamental operations of the PVT variation detector. The PVT variation detector consists of three blocks: delay line, digitizer, and switching detector. Open loop circuit of the delay cells formulates the delay line and the intention of the digitizer is to quantize the outputs of the delay cells. When the reference clock is fed to the circuit, multi-phase clock is generated with a constant phase difference between delay cells. The number of 'Hi' state outputs of delay line varies according to PVT variations. Digitizer using these multi-phase clock signals count the number of 'Hi' delay cell's outputs, and switching detector locates the place where input signal changes from 'Lo' to 'Hi'. Precisely, the switching detector spots the last 'Hi' delay cell. The output signal from the PVT variation detector is fed to the select signal generator to produce the appropriate control signals. These control signals are then utilized to control the slew rate of the output driver.

β ratio (W_p/W_n) of the delay cell is kept same as that of the segmented output driver shown in Fig. 3, to match the PVT variations between the control block and the output driver. Since the delay cells are constructed with static inverters, they consume less power. The number of delay cells is set to 20 in order to satisfy and locate all PVT variation ranges in a given design specification.

Operation of the digitizer shown in Fig. 2 is described below. Capturing the output of the delay cell at π phase indicates that the output signal is holding an arbitrary voltage between V_{dd} and ground. Digitizer quantizes this analog output from the delay cell into the digital value of "1" or "0" at the falling edge of clock signal. Moreover, inverters are used at output of each delay cell to prevent the load capacitance from changing when D flip-flops of the N-bit registers switch. As a result, the delay time of each delay cell will keep the constant value τ. The outputs of the digitizer are fed to the switching detector. A primary role of the switching detector is to seek the switching location of the reference clock by the process of NOR with the inverted signals from the digitizer.

The select signal generator depicted in Fig. 3 illustrates that it uses output signals from the PVT variation detector to create on and off signals to control the segmented output driver. Fig. 3 also shows the structure of the distributed and weighted output drivers. To keep the output impedance constant, three inverters (inv1, inv2, inv3) are selectively turned on according to the PVT variations while the first inverter is turned on by default. Moreover, six delay blocks are inserted in front of the inverters to prevent inverters from being turned on simultaneously, thus minimizing switching power noise. Inv1, inv2, and inv3 are turned on selectively by the signals that are generated by the select signal generator.

Measurement Results and Conclusion

Simulation waveforms for the output-on-demand is shown in Fig. 4(a) where the slew rate of the output driver is changed from 1.2V/ns to 2.4V/ns, one cycle after the clock signal is fed to the PVT variation detector. Also, the simulated slew-rate of the output signals in response to the multiple PVT variations (NN, FF, SS, 25℃ to 95℃, 1.8V) are shown in Fig. 4(b). The waveforms show that output slew-rate for input data signal ranges from 2.1V/ns to 3.6V/ns. The measured output driver slew rate of 2.86V/ns with four different supply voltages is also shown in Fig. 4(c).

Fig. 5 shows the Shmoo plot of the output driver, which illustrates that the right inverters among segmented inverters are selected to turn on for various PVT ranges. Voltage was subdivided into 17 values by varying ±2% of the normal voltage. Temperature range was also divided, by varying the temperature in 10℃ increment at a time, from 25℃ to 95℃. For example, the symbol d,2 shown in Fig. 5 for the PVT variation range at FF, 25℃, 1.44V indicates that default inverter and inv2 turn on to attain desirable slew rate in between 2.1V/ns~3.6V/ns. If the number of control signal is increased from 3-bit to 4 or 5-bit, a fine control is possible and then the range of slew rate will be narrowed.

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Die photo of the proposed output driver using 0.18μm CMOS process is shown in Fig. 6. The die area of the proposed slew-rate control block is 0.009mm^2. Table 1 shows the comparison results of the proposed output driver with the conventional output drivers. The proposed output driver control block consumes only 13.7pW/bps and occupies the least area compared to conventional output drivers. Also, the proposed output driver successfully overcomes the shortcomings of previous output drivers. First, the proposed output driver is implemented with digital circuits only. This not only enables low power design but also reduces the chip area. Moreover, excellent transplanting trait of this circuit allows it to be used widely in many memory chips without significant redesign for different process technologies. Second advantage of proposed output driver is that due to open-loop characteristics and optimal architecture only one cycle time is needed for correct locking. Hence, output-on-demand can be feasible and the slew-rate control block can be shut-down whenever necessary. Furthermore, no external resistance is needed to calibrate output resistance of the output driver, which reduces pin count as well. The advantages mentioned above thus make proposed output driver widely applicable in many high-speed memory and PCI bus applications.

References

[1] S.-H. Shin et al., JSSC, vol. 38, no. 7, pp. 1227-1233, Jul. 2003.
[2] T. Matano et al., JSSC, vol. 38, no. 5, pp. 762-768, May 2003.
[3] M. Bazes et al., 2004 ISSCC, pp. 486-487.

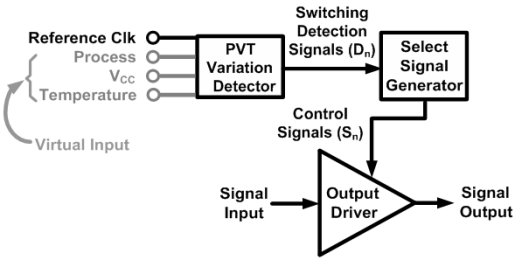

Fig. 1. Proposed slew-rate controlled output driver's block diagram.

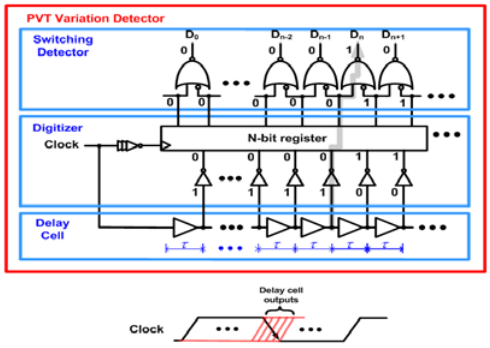

Fig. 2. The schematic of PVT variation detector and the operation of digitizer.

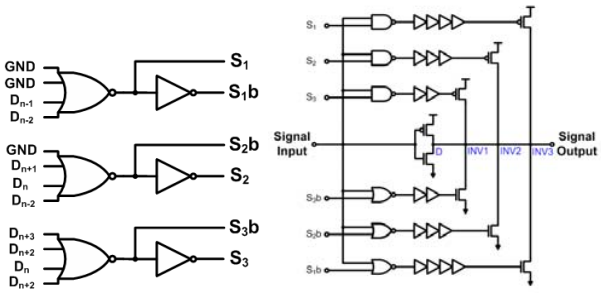

Fig. 3. Schematics of select signal generator and weighted output driver.

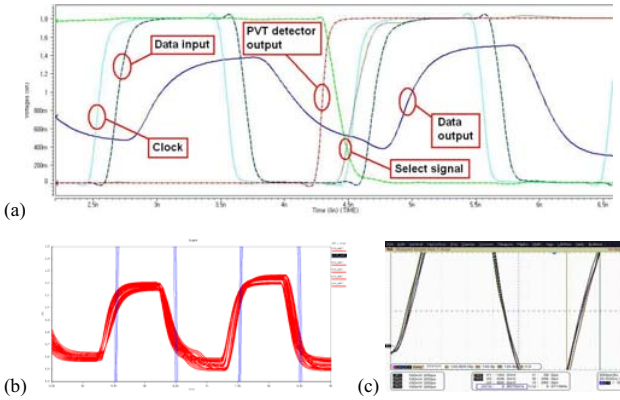

Fig. 4. Simulation results of output-on-demand (a) and constant slew rate with various PVT ranges (b) and the measured slew-rate with four different supply voltages (c).

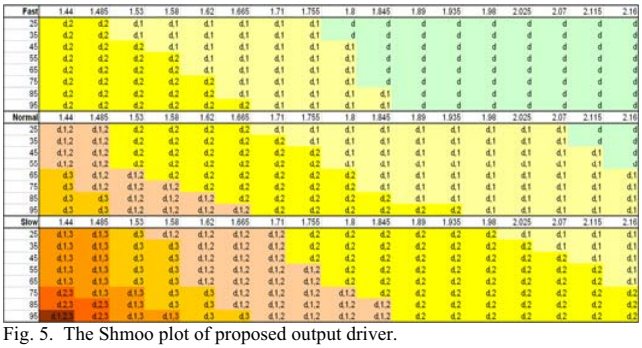

Fig. 5. The Shmoo plot of proposed output driver.

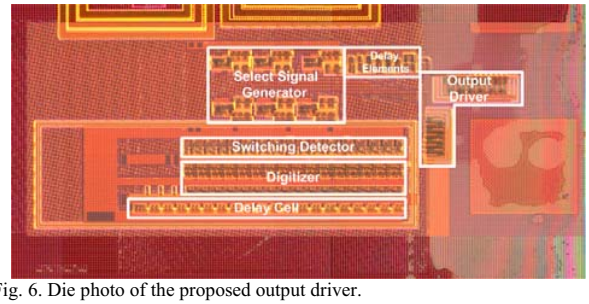

Fig. 6. Die photo of the proposed output driver.

Table 1. The comparisons of conventional and proposed output drivers.

	[1] S.-K. Shin JSSC 2003	[2] T.Matano JSSC 2003	[3] M.Baze ISSCC 2004	This work
Controller Type	Analog PLL	Mode/Digital Code	Digital SLL	Digital
Process	0.18um CMOS	0.13um CMOS	0.35um CMOS	0.18um CMOS
Operating Freq.	50Mbps	1Gbps	100Mbps	1Gbps
Power-down Mode	Difficult	Easy	Easy	Easiest
Lock Time	Hundreds of cycles	Tens of cycles	Several cycles	One cycle
Architecture	Close loop	Close loop	Close loop	Open loop
Slew Spec.	0.4–1 V/ns	2.0–4.0 V/ns	1.0–4.0 V/ns	2.0–4.0 V/ns
Measured Slew Rate	0.403–0.99 V/ns	1.6–2.2 V/ns	–	2.1–3.58 V/ns
Supply	3.3 V	1.8 V	3.3 V	1.8 V
External Resistance	–	Yes	No	No
Power Consumption	–	–	Medium (2.2mW, 0.22mW/Mbps)	Low (13.7mW, 0.013mW/Mbps)
Core Area	Large (0.16mm^2)	–	Medium (0.045mm^2)	Small (0.009mm^2)