A 1.2GHz Delayed Clock Generator for High-speed Microprocessors

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Abstract

A 1.2GHz delayed clock generator capable of adjusting its clock phase according to input clock frequencies has been developed. It consists of a full-digital CMOS circuit that leads to a simple, robust, and portable IP. One-cycle lock time enables clock-on-demand circuit structures. The implemented delayed clock generator tile in 0.13um CMOS technology occupies only 0.004mm^2 and operates at variable input frequencies ranging from 625MHz to 1.2GHz.

Introduction

Most microprocessors use PLLs as clock generators. However, a PLL is not suitable for low supply voltage operation and for clock-on-demand applications requiring fast lock time. To achieve a higher operating speed than the internal main clock frequency, multiphase clock can be used in large SoCs. However, large area is needed to distribute all of the multiphase clock signals through the entire die. In addition, skew and large power consumption become problematic. Local multiphase clock generation wherever it is needed overcomes these problems [2]. Although the mostly digital DLL in [1] and all-digital multiphase clock generator in [3] exhibit several digital design advantages they take up to 2.9μs and 128 cycles to be locked, respectively, which are not fast enough to achieve clock-on-demand. All-digital-circuit-based clock multiplication is also proposed with fast lock time of 1.3 cycles [4]. Small area, low power consumption, and fast lock time are important design parameters for local multiphase clock generators. In this work, a very compact delayed clock generator will be presented. The proposed delayed clock generator tile has two important features: open-loop non-PLL/DLL-based design and all-digital static-circuit-based design. The latter is good for portable IP and fast time-to-market designs. The former enables easy clock-on-demand schemes due to one-cycle lock time, smaller area, lower power consumption, no jitter accumulation, and lower voltage operation compared to PLL-based counterparts.

Architecture

Figure 1 shows the overall and detailed block diagrams of the delayed clock generator that consists of 1-to-0 transition detector, multiphase generator, phase interpolator, select signal generator, and multiplexer blocks. The chain of static inverter delay cells produces a series of the multiphase clocks (θ_1, θ_2,…, θ_n). The 1-to-0 transition detector senses the number of delay cell stages which have logic high states. The output signals of the detector cells (S_i) are fed into the select signal generator that is used for choosing the proper clock phase among the interpolator outputs (θ'_i). The phase interpolator generates two times denser clock phases than the raw delay chains. One of the fine grain signals is then selected and sent out to the output port by the selector block. If an output load is large, buffers can be utilized to drive the large load and that should be considered for proper signal selection.

Circuits and Operations

Operation of the 1-to-0 transition detector, which consists of a quantizer and an identifier, is explained in Fig. 1(b). The 1-to-0 transition detector senses π phase where the multiphase signals change from one to zero. Each quantizer consists of inverters and a positive edge-triggered D flip-flop. Since the outputs of delay cells are directly connected to the DFFs, the load capacitance of each delay cell can be varied according to each switching direction of DFF. Hence, an inverter is used to separate the two units, which enables the same delay amount (τ) for each delay cell at any given PVT conditions. Clock signal to DFF is delayed by three inverters: One inverter to match the inverter insertion delay for DFF data path and two inverters to guarantee (0.5τ+ setup time of DFF), where 0.5τ enables rounding off during quantization as shown in Fig. 1(b). The bottom left figure shows the actual capture point that is shifted by 0.5τ from π phase, which results in rounding off instead of rounding up. Since the phase of clock signal is inverted the DFF acts like a negative edge-triggered FF. The outputs of the quantizer feed to the identifier. It detects a point where the two inputs have different logic values, which means one of the identifier cells indicates the π phase point of the input clock. By this way, the select signals are generated by the 1-to-0 transition detector and one of the detector outputs (S_i) should be logic high.

Once 1-to-0 transition detector finds the position of π phase, the position of the π/2 phase can be easily determined since half the number of delay cells within the π phase is the position of π/2 phase. If the number of delay cells within a π phase is even the position of π/2 can be easily calculated. On the other case, if the number of delay cells within a π phase is odd, fine grain phases ($\theta'_{0.5}$, $\theta'_{1.5}$,…,$\theta'_{n-0.5}$) are needed. This is achieved by using a phase interpolator. The select signal should be adjusted to compensate the delay between the output of delay cell and final output clock as shown in Fig. 2. If the select signal points 3τ earlier, the delay amount of interpolator, multiplexer, and buffer can be offset. If τ is very long compared with the cycle time, the number of logic one's within π phase may be less than 6 at slow corner and the limitation of selection process is reached. To solve this problem, the repeated same clock phases are used for selecting the same clock phase as shown in Fig. 2(b). When τ becomes very long compared to cycle time, the multiple repeated phases (θ_i, θ_{3i}) are produced on a delay chain and one of them can be chosen using S_i and S_{3i}. This provides more design flexibility and accuracy. In this example, since the phase of θ_4 can be mapped to one of $\{\theta_{11}, \theta_{12}, \theta_{13}\}$, one of $\{\theta_{11}, \theta_{12}, \theta_{13}\}$ phases provides an accurate result. If θ_4 is mapped to θ_{12} as shown in the Fig. 2(b), θ_{10} is chosen instead of θ_2 and θ_7 is finally selected considering 3τ delay compensation.

Implementation

Using the proposed delayed clock generator, π/2 and 3π/2 phase generator tiles (108.5um×36.67um) are implemented in a 130nm CMOS process as shown in Fig. 3(top). The proposed delayed clock generator tiles are implemented in 14 places in a 1.2GHz RISC microprocessor as shown in Fig. 3(bottom). Multiphase generator tiles enabled pseudo-pipeline technique to be used in the 1.2GHz microprocessor, which makes many blocks of the microprocessor operate at like-2.4GHz performance with small power consumption increase. The extracted output load of each tile from the full-chip layout is normally 400fF. Because the delayed clock generator is designed for the operating frequencies ranging from 625MHz to 1.2GHz, seventeen delay cells were used to cover all PVT variations. Another test vehicle, tile2, running at 600MHz is fabricated in a 0.18μm process to get more precise test results of the proposed clock generator because the one in a 0.13μm process, tile1, is integrated in the RISC processor and no pin is assigned for it.

Measurement Results and Conclusion

Waveforms of tile1 are shown in Fig. 4. The upper waves show the original clock and its delayed phases. The middle waves are 1-to-0 detector output, select signal from the 1-to-0 select signal generator and selected phase (θ'_i). The final output clock is generated with a π/2 shifted phase with 1 cycle lock time. The phase errors ranged within ±2% of the cycle time. Figure 5 shows the measurement results from the test vehicle in a 0.18μm process, tile2. The left figure shows that the final output clock is generated with a π/2 shifted phase with 1 cycle lock time. The tile2 running at 500MHz has a peak-to-peak jitter of 7.6ps as shown in Fig. 5(right). Figure 6 shows the measured shmoo plot of tile2. The operating frequency range of the clock generator is from 200MHz to 600MHz within a ±2% phase error. It can operate up to 150MHz at halved supply voltage of 0.9V and consumes 0.5mW. Table 1 summarizes several digital multiphase clock generators. It shows that the proposed clock generator (tile1) occupies only 0.004mm^2, which enables local multiphase clock generation with only small overhead of area and power consumption. One cycle lock time is essential to return from power-down mode to active-mode for clock on demand operation so that it can be applied to voltage scaling microprocessors for low power operation.

Acknowledgement

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References

[1] B. Garlepp, et al., JSSC pp. 632-644, May 1999.
[2] K. Yamguchi, et al., 2001 ISSCC, pp. 398-399.
[3] A. Alvandpour, et al., 2003 ISSCC, pp. 112-113.
[4] T. Saeki, et al., 2000 ISSCC, pp. 166-167.

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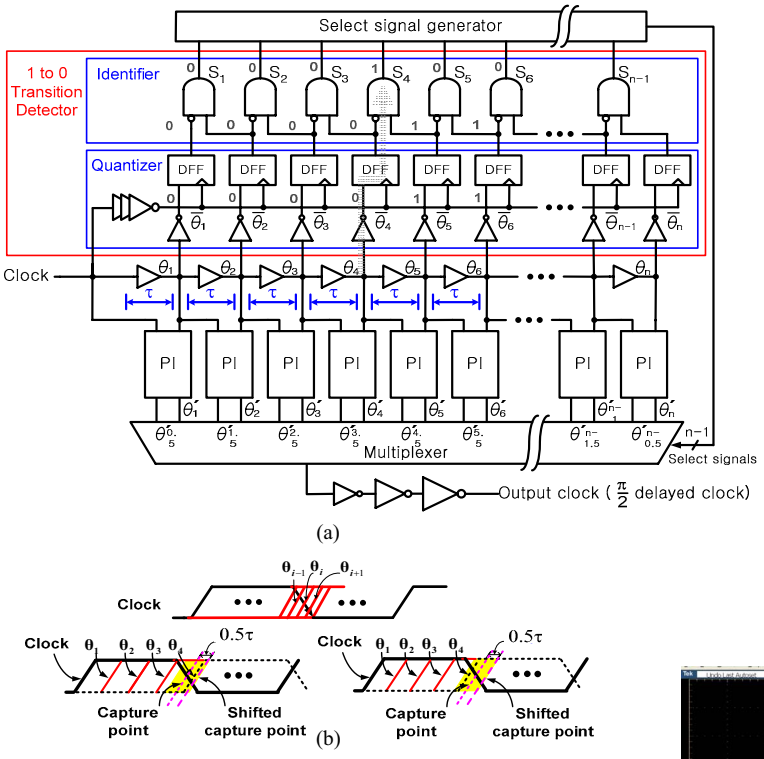

Fig. 1. (a)Overall block diagram and (b) operation of 1 to 0 transition detector.

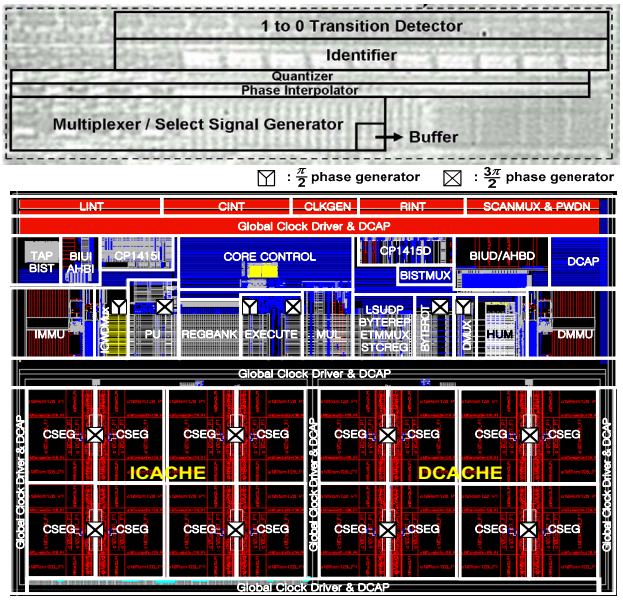

Fig. 3. Die photo of multi-phase clock generator in a 0.13μm process and its usages in the whole RISC microprocessor.

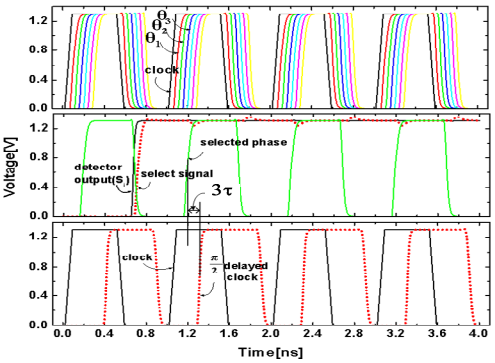

Fig. 4. Waveforms of clock phases, select, and output signals.

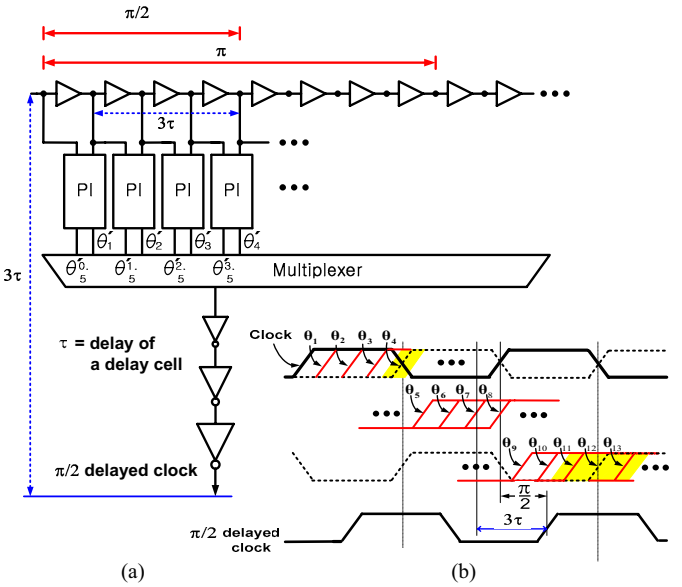

Fig. 2. Correct phase selection methodologies.

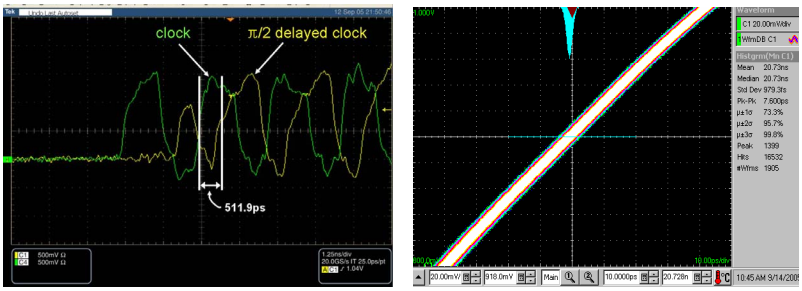

Fig. 5. Measurement results of multiphase clock generator in a 0.18μm process.

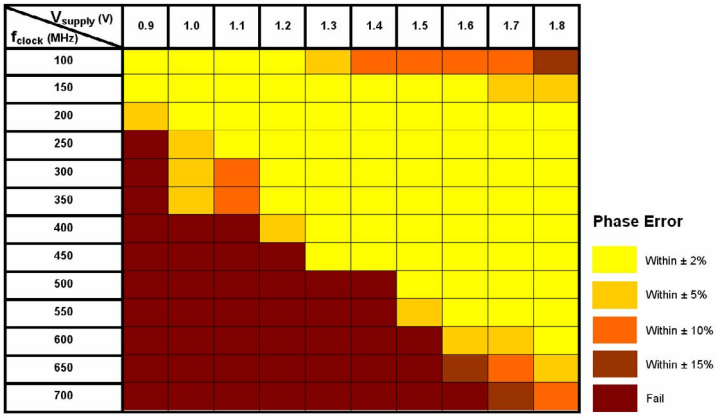

Fig. 6. Shmoo plot of the proposed delayed clock generator.

Table I. The comparisons of multiphase clock generators. * open loop, † closed loop

Company	Speed (GHz)	Process (um)	Area (mm^2)	Power (mW)	Supply (V)	Jitter (ps)	Phase error	Lock time
Rambus[1]	~0.667	0.4	0.96	340	1.7-4.0	245		2.9μs
NEC [2]	1.5 ~ 2.8	0.13	0.009	30	1.5	21* 46.8†	±5°	
Intel [3]	2.1 ~ 3.5	0.15	0.136	32* 70†	1.6		< 4%* < 8%†	128 cycle
NEC [4]	~ 1.2	0.25	0.140	15 @ 2.5V	0.9-2.5	400 @311MHz	0.29ns	1.3 cycle
Tile 1	0.625 ~ 1.2	0.13	0.004	3	1.2		< 2%	1 cycle
Tile 2	0.2 ~ 0.6	0.18	0.010	7.48	1.8	7.6@500MHz	< 2%	1 cycle
	0.05 ~ 0.15	0.18	0.010	0.518	0.9	30.8@150MHz	<2%	1 cycle

Note: [2] and [4] are clock and data recovery applications, and [3] and tile are for microprocessor applications.