Symmetry Constraint based on Mismatch Analysis for Analog Layout in SOI Technology

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Abstract – The conventional tools for mismatch elimination such as geometric symmetry and common centroid technology can only eliminate systematic mismatch, but can do little to reduce random mismatch and thermal-induced mismatch. As the development of VLSI technology, the random mismatch is becoming more and more serious. And in the context of Silicon on Insulator (SOI), the self-heating effect leads to unbearable thermal-induced mismatch. Therefore, in this paper, we first propose a new model which can estimate the combination effect of both random mismatch and thermal-induced mismatch by mismatch analysis and SPICE simulation. And in order to meet the different sensitivities of different symmetry pairs, an automatic classification tool and a configurable optimization process are also introduced. All of these are embedded in the floorplanning process. The final experimental results prove the effectiveness of our method.

I. Introduction

The variations in the parameters of two equally designed devices can be defined as mismatch. And it is seen as a limiting factor for the function and performance of analog circuits. In general, mismatch can be classified into two categories according to the different generating mechanisms: *fabricated-related mismatch* and *ambient-related mismatch*.

For the fabricated-related mismatch, there are two more detailed categories: (1) *systematic mismatch*; (2) *random mismatch*. Manufacturing variations results in device parameter variations from batch to batch, wafer to wafer and device to device. Batch-to-batch and wafer-to-wafer variations are common to all devices in the circuit. So, they are regarded as the systematic mismatch. And their effect on the circuit performance can be largely eliminated by layout techniques such as symmetry constraint. Therefore, the conventional tools for symmetry constraint [1]-[4] mainly aim at automatically placing the equally designed devices symmetrically with respect one or several common axes in order to eliminate the systematic mismatch. And we define these tools as *geometric symmetry tools*. Unfortunately, the existence of random mismatch weakens the ability of geometric symmetry tools in eliminating mismatch. Device-to-device variations which are defined as the random mismatch are caused by some unpredictable processes during design and fabrication phases. And random mismatch will greatly increase as the size of transistors decreases [12]-[14]. Nowadays, the size of transistor is in the magnitude of deep-submicron. As a result, the *random mismatch* will become more severe. This brings a great challenge for geometric symmetry tools to guarantee the matching constraint for the symmetrical devices.

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The *ambient-related* mismatch can be expressed as the mismatch caused by the ambient factors like thermal condition and noise distribution. Thermal-induced mismatch [6]-[8] is an important one in this kind of mismatch. Because of the relatively better thermal conductivity of the silicon [8], the thermal-induced mismatch is often neglected and the analog circuits are assumed as isothermal. However, in the context of SOI, the conductivity of isolating buried oxide is often over two orders of magnitude worse than silicon [9]. Thus, even with the relatively moderate power levels encountered in typical signal path transistors, increases in the channel temperature of tens of degrees due to self-heating effect can be observed [10]. And some of the heat generated by the distinct devices will flow laterally before reaching the substrate. So, the temperatures of these neighboring transistors will also rise. The temperature gradients resulting from self-heating and thermal coupling lead to nonisothermal conditions. Literature [11] is proposed to reduce the temperature gradient on symmetrical devices. However, its optimization objective is the *Minimum Average Temperature Gradient* (MATG) of all symmetry pairs. This method only aims at temperature optimization and ignores the different mismatch sensitivities of devices for different use and this may still lead to mismatch on some sensitive symmetry pairs.

Now there is no appropriate calculation model to estimate the combination effect of random mismatch and thermal-induced mismatch. The random mismatch model in [5] ignores the thermal factor and the accurate SOI models considering self-heating are time consuming. So, this paper first proposes a mismatch model for evaluating the combination effect of the two kinds of mismatch by SPICE simulation in Section II. Then in order to meet the different sensitivities of different symmetry pairs, an automatic classification tool and a configurable optimization process are introduced in section III. At last, all of these are embedded in the floorplanning process. The final experimental results are presented in section IV.

II. Mismatch Model Analysis

A. Random Mismatch Model

The random mismatch of two closely spaced, identical MOS transistors can be measured in terms of the variation in the drain current which is shown in (1) and has been extensively investigated down to deep-submicron device sizes [5] [12]-[14].

$$I_D = \beta[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \qquad (1)$$

The experimental data shows that the dominant sources for random mismatch are the variations in threshold

voltage V_T and current factor β ($\beta = \mu_n C_{ox} W/L$). In this paper, a widely accepted random mismatch model in [5] is used to calculate the random mismatch. According to this model, the variations in threshold voltage V_T in (2) and current factor β in (3) depend on the technology, the size of devices and the distance between the two devices.

$$\delta_R^2(V_T) = \frac{A_{V_T}^2}{WL} + S_{V_T}^2 D^2 \quad (2) \qquad \frac{\delta_R^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL} + S_\beta^2 D^2 \quad (3)$$

In these two equations, A_{VT}, S_{VT}, A_β and S_β are the technology-depended constants, they vary with different technologies. W and L stand for the gate-width and the gate-length respectively. And D is the distance between the symmetrical devices. Further more, the experimental data shows there is a low correlation between $\delta_R(V_T)$ and $\delta_R(\beta)$, and they can be modeled as two independent variables for I_D in (4).

$$\frac{\delta_R I_D}{I_D} = \sqrt{\frac{4\delta^2(V_T)}{(V_{GS} - V_{T_0})^2} + \frac{\delta^2(\beta)}{\beta_0^2}} \quad (4)$$

From this model, it is clear that the random mismatch will increase as the size of the devices decreases which is shown in Fig.1. As a result, the rising random mismatch weakens the ability of geometric symmetry tools to eliminate mismatch. Therefore, it is necessary to consider random mismatch on symmetrical devices in deep-submicron technology.

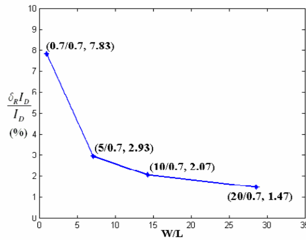


Fig.1 Random mismatch of different size in 0.7 technology

B. Thermal-induced Mismatch

In the context of SOI, the self-heating effect and floating body effect will also bring mismatch on the drain current. However, the mismatch caused by floating body effect can be greatly suppressed by *H-gate* layout [15], with both body contacts connected to the source or supply rails. Therefore, the thermal-induced mismatch becomes the dominant new mismatch source in SOI technology.

As power is dissipated in the channel of an SOI device, the localized temperature rises then affects the device's channel current mainly through the mobility and threshold voltage [10], which is shown in the following two equations.

$$V_T = V_{T0} - \lambda(T - T_0) \quad (5) \qquad \mu_n = \mu_{n0}(T/T_0)^{-k} \quad (6)$$

In (5), T_0 is the temperature of the ambient, V_{T0} is the threshold voltage at T_0 and λ is the threshold temperature coefficient with a typical value of -1~-3 mV/K [16] for NMOS devices. In (6), μ_{n0} is the effective mobility at T_0. And k is the mobility temperature exponent with typical value from 1.5 to 1.7 [16] for NMOS devices. And we assume that $C_{ox}W/L$ is a constant for a given device. Therefore, (6) can be converted to (7), in which β_0 is the current factor at ambient temperature.

$$\beta = \beta_0 (T/T_0)^{-k} \quad (7)$$

The combination of these effects leads to a reduction of drain current with rising channel temperature. We test this effect with a partially depleted SOI MOSFET model (the Southampton Thermal Analog or STAG model [10]) which is implemented in SPICE3. In Fig.2, a 20/0.7 device is tested with and without self-heating effect. It is clear that as the power ($P = I_D V_{DS}$) increases, an observable deviation in I_D can be detected. When V_{GS}=3V, over 5% mismatch can be observed and this is at the same magnitude as the random mismatch shown in Fig.1.

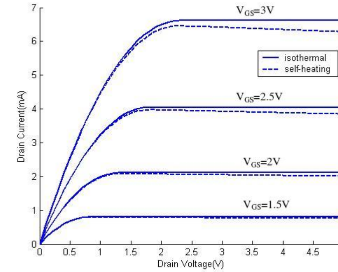


Fig.2 I-V curves with and without self-heating

Based on (5) and (7), the thermal-induced deviation in V_T and β can be easily calculated with the following two equations.

$$\Delta V_T = |\lambda(T_2 - T_1)| \quad (8)$$

$$\Delta\beta/\beta = |(T_0/T_2)^{-k} - (T_0/T_1)^{-k}| \quad (9)$$

The combination effect in I_D can be constructed by using (4). In order to distinguish these two kinds of mismatch $\delta_T I_D / I_D$ is used to denote thermal-induced mismatch in (10).

$$\frac{\delta_T I_D}{I_D} = \sqrt{\frac{4\Delta^2(V_T)}{(V_{GS} - V_{T_0})^2} + \frac{\Delta^2(\beta)}{\beta_0^2}} \quad (10)$$

The accuracy of this equation is also tested with SPICE3 on STAG model. The difference is so small that can be ignored.

C. Combination Mismatch Effect

In the context of SOI technology, the combination of these two kinds of mismatch mainly determines whether a symmetry pair is matching or not. In order to explore the way in which they incorporate together, the small-signal equivalent circuit method in [17] is used. With this method, a MOS device equals to the circuit in Fig.3. And it is clear that the device transconductance g_m is the sum of two parts: temperature-independent g_{m0} and temperature-depended g_{mT} in (11).

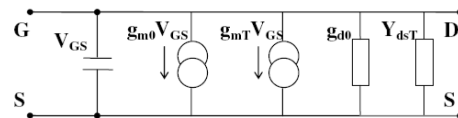


Fig.3 Small-signal equivalent circuit

$$g_m = g_{m0} + g_{mT} \quad (11)$$

For a given static operation point, V_{GS} is fixed. Therefore, the I_D mismatch is the sum of random mismatch and thermal-induced mismatch according to (12) and (13) in which I_{D0} is temperature-independent whereas I_{DT} is temperature-depended.

$$I_D = (g_{m0} + g_{mT})V_{GS} = I_{D0} + I_{DT} \quad (12)$$

$$\frac{\delta I_D}{I_D} = \frac{\delta_R I_D}{I_D} + \frac{\delta_T I_D}{I_D} \quad (13)$$

However, these two kinds of mismatch may have different "orientations". For example, for a given symmetry pair (Ma, Mb); the random mismatch causes I_D of Ma is larger than that of Mb. On the contrary, the temperature of Ma is higher than that of Mb, which causes I_D of Ma is smaller. As a result, these two kinds of mismatch are counteracted. Whereas, the random mismatch is unpredictable. Thus, the worst mismatch situation in (14) is chosen as the mismatch estimation formula in order to guarantee the performance of the symmetrical devices.

$$\frac{\delta I_D}{I_D} = |\frac{\delta_R I_D}{I_D}| + |\frac{\delta_T I_D}{I_D}| \quad (14)$$

III. Automatic Classification Tool and Configurable Optimization Process

A. Automatic Classification Tool

Different use of symmetrical pairs determines their different sensitivities to the mismatch. Therefore, it is improper to treat all the symmetrical pairs equally. For this reason, classification is necessary. In this section, several heuristic rules are introduced as the guidelines for the classification.

(a) In analog circuits, several MOS devices are treated as resistances by connecting their gate and drain together. These devices are very sensitive to mismatch, because they may lead to voltage gradient on signal processing devices. If the drain currents on them are different, the voltages on them will be different, too. For given *Vdd* and *Vss*, this may lead to different *Vds* on the signal processing pair. So these devices are of the highest priority.

(b) The mismatch requirement for symmetrical pairs in signal processing part is more rigorous than those in bias part. This is because signal processing part guarantees the function of the analog circuit, while bias part is used to supply reference current or voltage.

(c) For the symmetrical pairs in signal processing part, those in the first stage has a priority than others. For current processing signal systems, the accuracy of the system will be determined by the equivalent input offset voltage [18] which is shown in (15), where V_{osi} and A_i are the input offset voltage and gain of *i-th* step respectively.

$$V_{oseq} = \sqrt{V_{os1}^2 + (\frac{V_{os2}^2}{A_1}) + (\frac{V_{os3}^2}{A_1 A_2}) \cdots} \quad (15)$$

Based on the constraint generation method in [19], we can extract all the symmetry pairs and partition the circuit to several groups. In Fig.4 (M1a, M1b), (M2a, M2b), (M3a, M3b), (M4a, M4b) are symmetry pairs. The whole circuit is divided into five groups from G_1 to G_5. The schematic of the circuit can be converted into a connected graph CG = {(V, E)}, where V is the set of devices and E is the set of nets. The connected graph for Fig.4 is shown in Fig.5

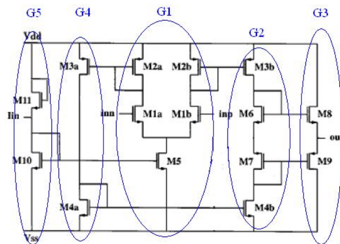


Fig.4 Schematic of a high-speed comparator

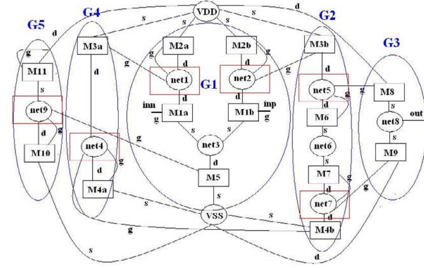


Fig.5 Connected graph for Fig.5

By defining *output net* of a group, CG can be simplified as a directed graph CG' = {(V', E')}, where V' is the set of groups and E' is the set of output nets. And the definition of *output net* is a net which connects several sources/drains in its group and only one gate in another group. And the *output net*s in Fig.5 are in the rectangles. With CG', the *signal path* which is defined as the shortest path from one input to its corresponding output can be determined. And with the three heuristic rules, the symmetry pairs can be classified into four levels: LV_1, LV_2, LV_3, and LV_4 automatically by searching CG. For the circuit in Fig.4, the signal paths for both inputs are $G_1 \rightarrow G_2 \rightarrow G_3$ and the results of classification are LV_1= {(M2a, M2b)}, LV_2= {(M1a, M1b)}, LV_3 is empty, LV_4= {(M3a, M3b), (M4a, M4b)}.

B. Configurable Optimization Process

The automatic classification tool is constructed according to the designers' experience. However, in some real cases, the priorities of these levels may change and sometimes not all the symmetrical devices are of the designers' interest. In order to make our algorithm more common, some configurable parameters are introduced into the optimization process. There are four parameters: k_1, k_2, k_3 and k_4 for LV_1, LV_2, LV_3 and LV_4 respectively. And the definition is as follows:

If k_i=1, (i=1, 2, 3, 4), every symmetry pair in LV_i should meet the designers' requirement. We call this "strong matching".

If k_i=0, (i=1, 2, 3, 4), there is no specific requirement for symmetry pairs in LV_i. The average optimization is the objective. And we call this "weak matching".

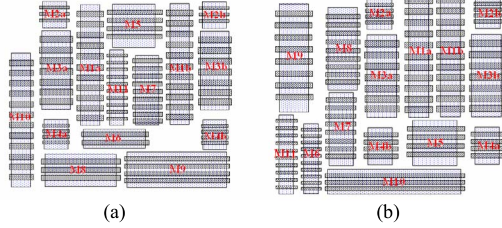
It is clear that if k_1= k_2= k_3= k_4=0, this algorithm degrades to MATG in [11]. And the matching limits and the values of k_i are given by the circuits' designers. If one symmetry pair in strong matching set overflows the limit, this solution is invalid. And the iteration of the valid solutions is driven by the average mismatch value in (16).

$$(\frac{\delta I_D}{I_D})_{avg} = \frac{1}{n}\sum_{i=1}^{n}(\frac{\delta I_D}{I_D})_i = \frac{1}{n}\sum_{i=1}^{n}[(\frac{\delta_R I_D}{I_D})_i + (\frac{\delta_T I_D}{I_D})_i] \quad (16)$$

IV. Experimental Results

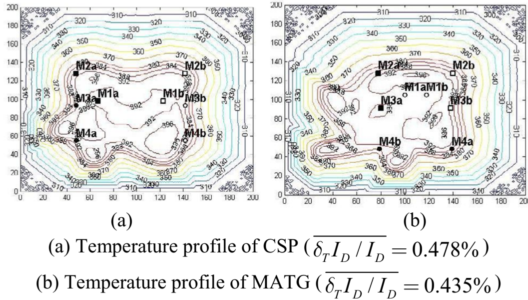
First, we compare our method which we call CSP (Classified Symmetry Pairs) with MATG in [11] using the instance in Fig.4 in which the four pairs are all in strong matching set. The numerical results are given in Table I. Fig.6(a) is the layout of CSP while Fig.6(b) is the layout of MATG. Fig.7(a) and (b) are the temperature profiles corresponding to Fig.6(a) and (b). From the table and these

figures, it is clear that MATG can provide us a smaller average temperature gradient on symmetrical devices. But this method may still lead to overflow for some pairs like (M2a, M2b) in this instance, because it treats all the symmetry pairs equally but neglect some mismatch-sensitive pairs. On the contrary, by treating symmetry pairs with different priorities, all the designer's requirements can be satisfied with CSP.



(a) (b)

Fig.5 (a) Layout of CSP; (b) Layout of MATG



(a) (b)

(a) Temperature profile of CSP ($\overline{\delta_T I_D / I_D} = 0.478\%$)

(b) Temperature profile of MATG ($\overline{\delta_T I_D / I_D} = 0.435\%$)

Fig.6 Temperature profiles of CSP and MATG

V. Conclusions

In this paper, we propose a model to meet the demand of evaluate the combination effect of random mismatch and thermal-induced mismatch by SPICE simulation. At the same time, according to the different sensitivities of different pairs, an automatic classification tool based on some heuristic rules is introduced. Both the model and the tool are embedded in the floorplanning process. The experimental results have proved that both performance and geometric constraints are promising.

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Table I. Comparison of CSP and MATG

Symmetry Pairs	Designer's Requirement	$\delta_R I_D / I_D$ (%)		$\delta_T I_D / I_D$ (%)		$\delta I_D / I_D$ (%)		Overflow?	
		CSP	MATG	CSP	MATG	CSP	MATG	CSP	MATG
(M1a,M1b)	2%	0.432	0.431	0.171	0.175	0.603	0.606	No	No
(M2a,M2b)	1%	0.869	0.867	0.103	0.572	0.972	1.439	No	Yes
(M3a,M3b)	3%	0.483	0.482	1.110	0.657	1.593	1.139	No	No
(M4a,M4b)	3%	0.717	0.716	0.527	0.342	1.244	1.058	No	No