Heuristic Power/Ground Network and Floorplan Co-design Method

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Abstract— It's a trend to consider power supply integrity at early stage to improve the design quality. In this paper, we propose a novel algorithm to optimize floorplan together with P/G network. Compared with previous methods, our algorithm can search the floorplan space more efficiently and therefore lead to better results. Further, we also propose a smart heuristic method to build P/G mesh grid with optimized topology. Experimental results show our method can speedup the floorplanning process by about 10 times and reduce the routing area of P/G network while maintaining the floorplan quality and P/G integrity.

I. INTRODUCTION

As technology scales to nanometer-regime, the gates numbers are increasing dramatically while the supply voltage continues to fall, both of which will lead to less voltage margin and higher current density. Also, all these problems make robust on-chip power delivery a challenging work. In contemporary high performance chip design, many metal resources are used for P/G network to reduce the voltage degradation. However, using up metal resources for P/G network makes other design components, such as clock networks, hard to design. In this case, this problem could lead to several design iteration. So it's important to fix the power supply problem as early as possible. This requirement makes early-stage P/G network design necessary.

Recently, it's a trend to co-synthesis the power supply network at early design stage, e.g. P/G network co-synthesis with floorplan [1–4]. These co-synthesis methods can improve the power design quality and reduce the design iteration dramatically. This early-stage co-synthesis design methodology allows the designer to adjust the positions of underlying gates, which act as 'power consumers', with design parameters of P/G network simultaneously, in contrast to traditional power supply network design flow, where only design parameters of P/G network can be adjusted and the positions of underlying gates are fixed. So we could have more design choices and pick up a better quality one in co-synthesis design process.

If we analyze these presented co-synthesis algorithms, we will find that all of them actually handle three key problems. The first one is how to compute the voltage drop of P/G network efficiently for variant floorplan. The second one is how to adjust the floorplan to reduce voltage drop. And the third one is how to optimize the P/G network topology to provide best power distribution using limited metal resources. However, due to the complexity and individual characteristics of floorplan and P/G network topology optimization, there are still lots of limitations in the presented algorithms. Among the existing problems, there are two severest ones. The first problem is how to estimate the voltage IR drop effectively in each floorplan iteration. Because there could be thousands of iterations during the floorplanning process, a slightly slower IR drop simulation will degenerate the overall performance of co-synthesis seriously. The second problem is how to integrate the floorplan optimization with P/G topology optimization seamlessly to provide more possible design choices are the most important ones. In fact, [1] and [2] haven't discussed these issues sufficiently while [3, 4] emphasize on the reduction of decap area instead of design of optimal power supply network. In paper [1], the P/G network is prescribed to be a uniform regular mesh network and the worst IR drop is obtained by solving a linear system. However, according to our experiments, the time used to build and solve this linear system in floorplan stage will lead to a obvious time overhead when the design is very large. Further, ignoring the irregular P/G topology could be a potential problem which could lead to miss of better design at early design stage.

In this paper, we propose a novel heuristic design method to integrate the P/G topology optimization into the floorplanning process. This heuristic method includes two parts. First, we introduce a "virtual metal plane" (VMP) for the IR drop estimation of given floorplan. The "virtual metal plane" is just a conceptual power supply system only for IR drop assessment, although some high-performance chips, such as Compaq Alpha processor [5], adopt "real" dual power plane as the power supply system. This "virtual metal plane" has the power supply function similar to a very dense mesh network. Because we could obtain the analytical solution to the "virtual metal plane", then it's proper to integrate this analytical solution that represents the power supply degeneration effect into floorplan process. After this part is done, we could have a good quality floorplan in both traditional criterion and power supply capability. The second part of the heuristic method is to construct a realistic power supply mesh network with optimal topology. This heuristic is illuminated by the topology optimization problem in isotropic material structure design [6]. We will remove the regions of "virtual metal plane" where little current is conducted and form a non-uniform power supply mesh network. Since removed regions conducted little current from pad to underlying gates, the power supply performance will be degrade slightly and the routing resources for power supply system

could be reduced largely. In summary, we first choose a suitable floorplan and then build a optimized non-uniform power supply mesh by our method. Due to the efficiency of analytical solution, the time cost of each iteration in floorplanning process could be reduced sufficiently. According to our experiments, the analytical method could lead to about 10 times speed-up comparing with linear system simulation method. At the same time, the power supply capability of the non-uniform P/G network obtained by our method is better than the simple regular mesh network.

Notice that we only consider the DC IR drop in this method for following reasons: (1) At early stage, the dynamical signature of block may be unknown [7] and IR drop could be regarded as a up-bound to the overall voltage drop. (2) As suggested by [8], there is little on-chip inductance impact in the contemporary design.

The remains of this paper is organized as follows. In section II, we present the principle of virtual metal plane concept which could estimate the IR drop efficiently. Section III formulates the floorplan and P/G network co-optimization problem; section IV presents our analytical estimation method for P/G network. V shows the heuristic method for P/G network topology optimization. In section VI, the co-synthesis algorithm for floorplan and P/G network is described. Finally, section VII shows the experimental results while section VIII gives the conclusion.

II. PRINCIPLE OF VIRTUAL METAL PLANE

Inspired by the metal plane power supply system in practice [5], we introduce the "virtual metal plane" (VMP) for the IR drop estimation. Although the metal plane is too expensive for many chips to adopt, it could be used for computational purpose. i.e. We could use it to assess the impact of the underlying blocks of floorplan to power supply system. Because the metal plane is not really allocated on the chip, so it's called "virtual" metal plane. An important reason we introduce the VMP concept is that we can obtain the analytical solution to the metal plane power supply system. For variety floorplans, the analytical solution facilitates quick determination of their impact to the power supply system, i.e. the IR drop. We will detail the analytical solution in section IV.

The feasibility of VMP solution depends on the fact that the metal plane, as power supply system, behaves similarly as the mesh grids. We argue that the analytical solution of VMP is conformable to the simulation results of mesh grids. We could verify this conclusion via the numerical analysis method for continuous metal plane. Fig. 1 shows a virtual metal plane and a mesh grid. As we will elaborate in section IV, the metal plane could be described by a PDE (Poisson Equation) which could be solved numerically by Finite Difference Method (FDM). To apply FDM we first need to discretize the metal. It is apparent the mesh grid resembles the discretized metal . Then both discretized metal plane and mesh grid form a linear system to solve. Through similarity of the metal plane and mesh grid, we could expect that they behave quite similarly. Because the discretization of metal plane induces some error comparing to the exact analytical solution, the solution of mesh grid is definitely not identical to analytical solution of metal plane and the error

or difference between mesh grid and metal plane depends on how dense the mesh grid is, i.e., the pitch p of mesh grid. By applying error analysis of multigrid method, we could obtain another important property that this error is $O(p^2)$ order and realistic mesh grids in contemporary chip is dense enough inducing tolerable error, which will be illustrated by experiments in section VII. Moreover, this error is also known as "high-frequency" error. That is, the obvious error occurs at regions where mesh grid doesn't cover.

So it's reasonable to use VMP approach to estimate the performance of power supply system and this approach largely benefits the computing efficiency.
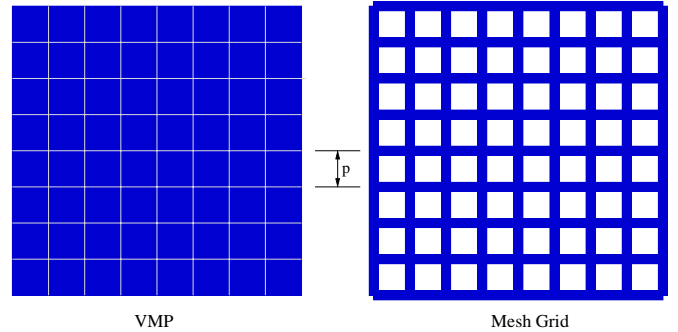

Fig. 1. Virtual Metal Plane VS. Mesh Grid

Another application of virtual metal plane is to serve as the guideline of P/G network design. Fig. 2 is the portrait of the current distribution on a metal plane. The left subfigure is the X-direction current component, i.e., current running horizontally. The right one is the Y-direction current component. Then we allocate power strips to cover the "hot spots" on the plane. This method will be elaborated in section V.

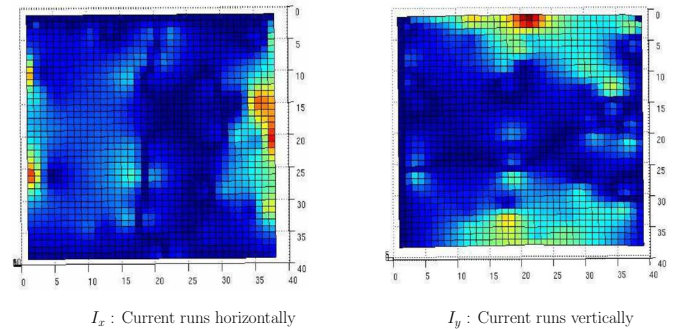I_x : Current runs horizontally I_y : Current runs vertically

Fig. 2. Current Distribution on Virtual Metal Plane

III. PROBLEM FORMULATION

Fig. 3 shows a typical mesh structure with power trunks, peripheral pads and core ring. We illustrate our formulation in aid of this figure. Usually, power trunks are routed horizontally and vertically in different metal layer, and the cross-nodes are named "P/G nodes". The underlying rectangles shown in Fig. 3 represent the floorplan blocks, each of which has one or several
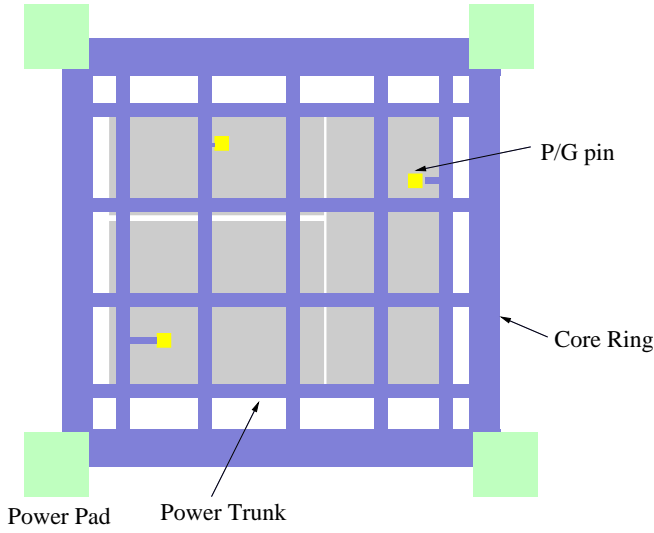
Fig. 3. Power Supply Network

pins connected to the power trunk or the core ring to get power.

Since floorplan is a $\mathcal{NP}\ Hard$ problem, heuristic methods such as simulate annealing(SA) are widely used as the solving engine. In order to integrate the P/G network optimization process into the floorplan stage, there also should be a cost function to represent the power supply performance.

In our formulation, the overall cost function contains three terms. The term A is used to describe the floorplan area, the term W is used to describe the total wire length, and the term R represents the metal resources used by P/G network in the constraint of worst voltage drop tolerance.

$$\min_{s} \quad \lambda_1 A(s) + \lambda_2 W(s) + \lambda_3 R(s) \qquad (1)$$
$$\text{where} \qquad \sum_{i=1}^{3} \lambda_i = 1$$

And for a given floorplan s, the metal resource $R(s)$ is defined as follows:

$$\min_{w,p} \qquad \{R = \sum l_i w_i\} \qquad (2)$$
$$s.t. \quad V_{wst} \le V_t, D_{max} \le D_t$$

where V_{wst} is the worst voltage drop, V_t is the voltage drop tolerance, D_{max} is the max branch current density, and D_t is the branch current density tolerance representing Electrical Migration (EM) constraints and l_i , w_i are the lengths and widths of power lines, respectively.

In paper [1], the cost function is proposed as follows:

$$\min_{s} \quad \lambda_1 A(s) + \lambda_2 W(s) + \lambda_3 \Phi(s) + \lambda_4 \frac{A(s)}{p_0^2} \qquad (3)$$
$$\text{where} \quad \Phi(s) = \theta \frac{|B_{em}|}{|B|} + (1-\theta)\frac{\sum_{n \in N_v} v_{n,v}}{\sum_n V_t}$$
$$G(p_i, w_j)v = I(s)$$
$$\sum_{i=1}^{4} \lambda_i = 1$$

where function $\Phi(s)$ represents cost function of the voltage drop and EM constraints and $\frac{A(s)}{p_0^2}$ corresponds to routing resources for P/G network (For more detailed explanation of this cost function, please see paper [1]). This formulation is different from our formulation (1). The reason is that if we allocate enough routing resource to P/G network, then the worst voltage drop can be reduced under the predefined threshold, and no voltage violation nodes will be found. This means Φ function in (3) is zero if R is solution of problem (2). Therefore, just adding term R defined in (2) to the overall cost function has the same effect as the Φ function in equation (3).

IV. ANALYTICAL P/G NETWORK PERFORMANCE ESTIMATION

In order to solve the co-synthesis problem (1), we use the simulate annealing(SA) to search optimal solution. Because there are numerous iterations in SA process, it's critical to calculate the power supply cost function $R(s)$ very quickly for each floorplan s.

In order to calculate term $R(s)$ defined by formula (2), the traditional way is to construct a initial P/G network topology, then establish a linear system, next solve it, finally do some optimizations to reduce the metal resources $R(s)$. However, this process is too time consuming to fit in the SA process. To speed up the P/G network performance estimation, one way is to adopt a uniform mesh P/G grid as in [1]. However, a uniform mesh could lead to excessive R because of its fixed topology and identical wire widths. Our approach is to find R for a general non-uniform P/G network. In our strategy, we first suppose conceptually a whole metal plane, called "virtual metal plane" is allocated as the power supply system.This virtual metal plane resembles a very dense mesh network with R equal to whole die area. Therefore the power distribution capability of the metal plane is a upper bound of the mesh power grids. We then regard this very dense mesh network as a approximation of the solution to problem (2) and calculate the corresponding approximate optimal R, which will be plugged into problem (1). Then for different floorplans, we obtain different impacts to power supply degeneration by analyzing the virtual metal plane with given floorplan. Then we could choose an optimal floorplan with trade off between die-area, wire-length and power supply degeneration by solving problem (1).

Then we will show how to solve the "virtual metal plane" power supply system analytically. According to the Kirchhoff's law and Ohm's law, the voltage distribution and the current distribution of this metal plane can be calculated by the analytical result of a specific Poisson Equation. Suppose the die area is $\Omega = [0,a] \times [0,b]$, then the metal plane could be described by Poisson Equation defined on Ω. Because the practical P/G network usually has a "core ring" with relative large wire width comparing with other trunks, the voltage distribution in the "core ring" will be very close to V_{dd}, thus, it's reasonable to formulate the boundary conditions as Dirichlet Condition. So the complete PDE is shown as follows:

$$\Delta \cdot V(x,y) \quad = \frac{I_0(x,y)}{\sigma} \quad (x,y) \in \Omega \qquad (4)$$

BCs :

$$V(x,y) \quad = V_{dd}(x,y) \ \ (x,y) \in \partial\Omega$$
$$\Omega \quad = \{(x,y)|0 \le x \le a, 0 \le y \le b\} (5)$$

where Δ is the Laplacian operator, σ is the conductivity and $\partial\Omega$ is the boundary of region Ω.

Moreover, the current function I can be formulated by the delta function as below:

$$I_0(x,y) = \sum_{k=1}^{N_b} I_k \delta(x_{k_i}, y_{k_i})$$

where N_b is the number of blocks, I_k is current absorbed by block k, $\delta()$ is the Dirac delta function, and (x_{k_i}, y_{k_i}) are the power pin positions of the kth block. According to solution of equation (4) represented by Green's function, the analytical voltage distribution will be given by formula (6).

$$V = \frac{4}{\sigma ab} \sum_{k=1}^{N_b} \sum_{i=1}^{\infty} \sum_{j=1}^{\infty} I_k \frac{\sin(p_i x)\sin(q_j y)\sin(p_i x_k)\sin(q_j y_k)}{p_i^2 + q_j^2}$$
(6)

where $p_i = \frac{\pi i}{a}$ and $q_j = \frac{\pi j}{b}$. This approximation to this analytical solution could be obtained by limit i and j from 1 to not very large integer. The numerical simulation results proves that this approximation is accurate enough.

In order to obtain the routing resource resource $R(s)$ for a given floorplan s, we first build the right-hand-side (RHS) $I_0(x,y)$ based the positions of pins of floorplan s. Then we calculate the voltage drop V by applying analytic formula (6). Then we could estimate the required routing resource by scaling the voltage drop to threshold V_t. Because the voltage drop is inversely proportional to routing resource, the scaled metal resource is the routing resource required to satisfy the power supply integrity, which could be calculated by (7).

$$R(s) = \frac{a \times b \times V_t}{||V||_\infty}$$
(7)

Plugging equation (7) to problem (1), we could then use SA method to search for optimal floorplan s^*

V. Topology Optimization of P/G Network

The second part of our algorithm is to construct a non-uniform P/G mesh network with optimized topology for the chosen floorplan s^*. Since we already have the voltage and current distribution of "virtual metal plane", we could carry out the topology optimization as introduced by [6]. The basic idea of this topology optimization is to remove the regions where the current density is low. Because the cropped regions have conducted little current, removing these regions will cause minimal power supply degeneration. Moreover, the optimized P/G network should be a mesh network for manufactural reason, i.e. a mesh network is formed by removing the "useless" metal from the "virtual metal plane".

Then we will detail this heuristic method for topology optimization of P/G network. Once the voltage distribution obtained, we can calculate the current distribution using Ohm's Law, according to which we will plan our P/G network with promising performance. Since the metal lines of P/G networks run horizontally and vertically, we could project the two dimension current density of metal plane into either horizontal or

vertical direction to accord with the practical design. Here we use the following formulation:

$$I_{px}(y) = \int_0^a \sigma |\frac{\partial V}{\partial x}|\,dx$$
(8)
$$I_{py}(x) = \int_0^b \sigma |\frac{\partial V}{\partial y}|\,dy$$

This integration of current density can represent the line current in a horizontal(vertically) layer. According to the value of the current distribution, we could allocate more metal in the "hot spots", i.e. places wider metal lines where current density is intense.

Algorithm 1 summaries the heuristic method of topology optimization of P/G network.

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1 Construct current function $I_0(x,y)$ according to module's position
2 Solve the equation (4)
3 Calculate the current map according to equation (8)
4 Allocate metal lines, satisfying
$\int_{y_i}^{y_i+p_i} I_{px}(y)\,dy = \int_{y_j}^{y_j+p_j} I_{px}(y)\,dy$, where p_i is the ith pitch
5 Determine the ratio between wires according to
$\frac{w_i}{w_j} = \frac{\int_{y_i}^{y_i+p_i} I_{px}(y)\,dy}{\int_{y_j}^{y_j+p_j} I_{px}(y)\,dy}$
6 Given a unit routing resource R_0 for P/G net, set wire widths to be $\frac{R_0}{l_i}\frac{w_i}{\sum w_i}$
7 Simulate the P/G network and obtain the worst IR drop V_{wst} and max branch current density D_{max}
8 $r \leftarrow \max\{V_{wst}/V_t, D_{max}/D_t\}$
9 $R(s) = r \cdot R_0$

Algorithm 1: Heuristic Design Algorithm.

VI. Floorplan and P/G network Co-optimization Algorithm

As mentioned before, the whole co-synthesis strategy we proposed consists of two key parts: 1. analytical estimation to power supply degeneration; 2. topology optimization of P/G network. What we need to do is to combine this two parts properly and integrate these parts to SA optimizing engine. So we finally give our P/G network and floorplan co-optimization as algorithm 2.

VII. Experimental Results

Algorithms are implemented in C++ and tested in Linux box with 2.8 Hz CPU and 1G main memory. We apply our algorithms to the MCNC benchmarks.

We first illustrate the conformity between analytical solution to metal plane and simulation results of mesh grid. In order to find out the correlation between metal plane and mesh grid, we first build a metal plane and a 20×20 mesh grid covering the same die area. Then we place 49 underlying blocks connecting to metal plane and mesh grid, respectively. Next we permute

```
while T > T_min do
    Normalize the cost
    Initial the floorplan s
    s* ← s, Ψ* = Ψ(s)
    for i =1 to n do
        Perturb floor plan: s' ← perturb(s)
        Calculate the area and wire-length A(s'),W(s')
        Calculate R_s' using equation (7)
        Calculate the cost function
        Ψ(s') = λ₁A(s) + λ₂W(s) + λ₃R(s)
        ΔΨ = Ψ(s') − Ψ(s)
        if ΔΨ ≤ 0 then
            s ← s'
        end
        else
            s ← s' with probability e^(−ΔΨ/T)
        end
        if Ψ(s') < Ψ* then
            s* ← s'
            Ψ* ← Ψ(s')
        end
    end
    T = rT
end
For best floorplan s*, apply algorithm 1 and set its result to
R*
```

Algorithm 2: SA Process for Co-optimization

the positions of underlying blocks for 100 times and we compute the worst IR drop for each permutation in both metal plane and mesh grid cases, i.e. V_{pl} : worst IR drop by solve VMP analytically and V_m : worst IR drop in mesh grid by simulating linear systems. At last we plot V_{pl} versus V_m, as shown in Fig. 4. We could see that these two estimation is consistent, i.e. larger V_{pl} indicates larger V_m. As we mentioned in section II. V_{pl} is not identical to V_m because of the discretization error. However, we could say that V_{pl} is conform to V_m at large.
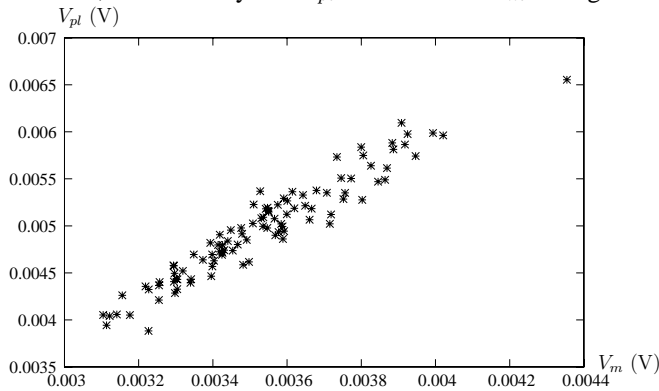

Fig. 4. V_{pl} $VS.$ V_m

Then we demonstrate performance of co-optimize algorithm 2 by table I. The "Area" and "HPWL" columns are the area and wire length of floorplans, respectively, which are presented to show the trade-off between traditional floorplan and power supply performance. As we mentioned before, another important criteria is the necessary P/G routing area satisfying the IR drop and EM constraints. We compare the P/G routing are in three cases: The first case is the "plain floorplanner", which executes traditional floorplanning without considering the impact of blocks to power supply and just adopt a uniform mesh to satisfy the power supply constraints after floorplanning. The second case is the "Uni-mesh Based Floorplanner", which considers the impact of blocks to power supply in floorplanning process while also uses a uniform mesh to meet the power supply requirements. The third case is the "Plane Based Floorplanner", which considers the impact of blocks to power supply in floorplanning process by VMP method and finally build a non-uniform mesh to satisfy the power supply constraints. Because the routing resource of the mesh grid in these cases is the criteria to judge the quality of P/G network planning, we compare the routing resource of the routing area of final mesh grid built in these cases (uniform mesh in the first and second cases and non-uniform mesh in the third case) as following: The A_p column under "plain floorplanner" represents the P/G routing resource satisfying the IR drop and EM constraints in the traditional floorplanning. Column ΔA under the "Uni-mesh Based Floorplanner" is the P/G routing resource reduction percentages of uniform mesh built in second case with respect to routing resource in the plain floorplanner case, i.e. $\Delta A = A_{uni}/A_{plain} - 1$ and column ΔA in the "Plane Based Floorplanner" is the P/G routing resource reduction percentages of non-uniform mesh built in the third case with respect to the plain floorplanner case, i.e. $\Delta A = A_{non-uni}/A_{plain} - 1$. We could see that both "Uni-mesh Based Floorplanner" and "Plane Based Floorplanner" can reduce the routing resource of P/G network because they consider the impact of floorplan to power supply network. Also we could see the "Plane Based Floorplanner" is $1X$ time faster than the "Uni-mesh Based Floorplanner" and it reduces the routing resource more than "Uni-mesh Based Floorplanner" because it uses the general non-uniform mesh.

VIII. CONCLUSION

Finding a good floorplan in terms of several criteria is a challenging job because it's either too time-consuming or unable to find the optimal solution. In this paper, we propose a new floorplan and P/G network co-optimization method to find a promising floorplan which benefits the power supply integrity. By introducing the analytical VMP approach, we estimate the power supply capability efficiently. As a consequence, we speedup the floorplanning process. We also propose a novel heuristic P/G design method to carry out the fast P/G topology optimization with the given floorplan and the non-uniform mesh grid built by this method saves the routing resources of P/G network further more. So if other components, such as clock network, compete intensely with the power supply system for the routing resources, our method could be a good choice to alleviate the resource problem. Future work will pay attention to the transient model of the floorplan and the corresponding co-optimization problem.

Module	Plain Floorplanner				Uni-mesh Based Floorplanner				Plane Based Floorplanner			
	Area (mm^2)	HPWL (mm)	A_p (mm^2)	Time (s)	Area (mm^2)	HPWL (mm)	ΔA %	Time (s)	Area (mm^2)	HPWL (mm)	ΔA %	Time (s)
apte	50.07	718.83	1.86	0.144	48.2	682.9	-32.1%	19.77	50.06	675.6	-63.1%	0.84
hp	9.55	191.4	1.08	0.424	11.66	199.3	-40.4%	30.47	11.59	162.5	-41.6%	3.24
ami33	1.29	76.05	0.135	2.57	1.30	96.47	-59.7%	95.14	1.28	87.04	-69.2%	12.78
ami49	39.60	1006	13.80	6.4	39.90	1282	-65.1%	138.97	40.30	1160	-69.4%	27.68
xerox	20.33	381.18	1.88	0.328	21.2	426.9	-48.0%	20.53	21.71	460.34	-53.7%	1.44

TABLE I
EXPERIMENTS ON MCNC BENCHMARKS

REFERENCES

[1] C.-W. Liu and Y.-W. Chang, "Floorplan and power/ground network co-synthesis for fast design convergence," in *Proceedings of the 2006 international symposium on Physical design*, 2006, pp. 86–93.

[2] S.-W. Wu and Y.-W. Chang, "Efficient power/ground network analysis for power integrity-driven design methodology," in *Proceedings of the 41st annual conference on Design automation*, jun 2004, pp. 177–180.

[3] I.-M. Liu, H.-M. Chen, T.-L. Chou, A. Aziz, and D. Wong, "Integrated power supply planning and floorplanning," in *Proceedings of the 2001 conference on Asia South Pacific design automation*, 2001, pp. 589–594.

[4] S. Zhao, K. oy, and C.-K. Koh, "Power supply noise aware floorplanning and decoupling capacitance placement," in *Proceedings of the 2002 conference on Asia South Pacific design automation*, 2002, p. 489.

[5] B. Herrick, "Design challenges in multi-ghz microprocessors," in *Proceedings ASPDAC 2000*, 2000.

[6] M. P. Bendsoe and O. Sigmund, *Topology Optimization Theory, Method and Applications*. Springer, 2003.

[7] A. Dharchoudhury, R. Panda, D. Blaauw, R. Vaidyanathan, B. Tutuianu, and D. Bearden, "Design and analysis of power distribution networks in powerpc^{TM} microprocessors," in *Design Automation Conference (DAC'98)*, jun 15-19 1998, pp. 738–743.

[8] S. Pant and E. Chiprout, "Power grid physics and implications for cad," in *Proceedings of 2006 Design Automation Conference*, 2006, pp. 199–204.