Analytical Model for the Impact of Multiple Input Switching Noise on Timing

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***Abstract*— The timing models used in current Static Timing Analysis tools use gate delays only for single input switching events. It is well known that the temporal proximity of signals arriving at different inputs causes significant variation in the gate delay. This variation in delay affects the accuracy of our timing estimates. In this paper, we derive simple analytical models for incorporating the effect of simultaneous multiple input switching events on gate delay. The model presented requires minimum additional characterization effort, and can be employed in a statistical timing engine. The dynamic delay variability of a path caused by MIS noise can be accurately estimated using the proposed model.**

I. Introduction

Timing libraries used by static timing analysis tools have pin-to-pin delays of each gate characterized for Single Input Switching (SIS) events only. Ignoring the delay effects caused by simultaneous switching of multiple inputs has been known to introduce significant errors in timing estimates [1]-[6]. The Multiple Input Switching (MIS) effect has largely been evaded during both static and dynamic timing analysis due to the complexity in delay characterization. In this paper, we derive a simple model for estimating MIS error for basic logic gates that does not require extensive characterization since it is based primarily on the SIS delays which are already present in the timing libraries. The model can be used for estimating dynamic path delay variation during critical path selection for delay tests, or for more accurate dynamic timing simulation.

A signal transition at the input of any basic logic gate can either be a *Controlling to Non-Controlling* (CTN) or *Non-controlling to Controlling* (NTC) depending on its effect on the output. For any gate, the controlling value is the one that enables one of the parallel current paths, either pull-up or pull-down, to the output node. For a NAND gate, the controlling value is 0; hence a rising transition is a CTN transition while a falling transition is NTC. In general, when only one of the inputs is switching and all the other inputs take a non-controlling value, the pin-to-pin delay can be called the SIS delay. The MIS delay needs to be considered when more than one input make a transition in the same direction. If the inputs are switching in opposite directions, then either there is a glitch at the output (if the CTN transition arrives before the NTC transition), or no signal is propagated to the output. In this paper, we do not model the delay effect due to glitch conditions. When multiple inputs have NTC transitions, the earliest arriving signal determines the output arrival time, while for CTN transitions at the inputs, the latest arriving signal determines the output arrival time. The following two sections derive analytical models that estimate the output arrival time of a gate considering MIS efffect.

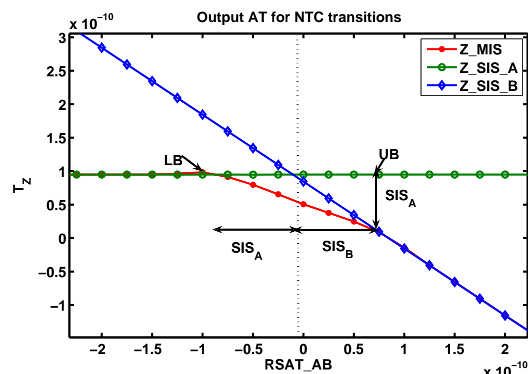

Fig. 1. MIS effect on A for NTC transition

II. MIS modeling for NAND2 gate

The *Arrival Time* (AT) at any node A is given by T_A. For a 2-input NAND gate, $Z = NAND(A, B)$, $T_Z^{S_A}$ is the AT at Z when only A is switching, i.e., the SIS case, while T_Z^M is the AT at Z when both the inputs are switching, i.e., the MIS case. We define the propagation delay from input A to output Z when only A is switching as $\Delta T_Z^{S_A}$. The impact of MIS on the propagation delay from A to Z is given by $\Delta T_Z^{M_A} = (T_Z^M - T_Z^{S_A})$. Since in the MIS case any of the two inputs could be dominant, we measure the output AT (T_Z).

A. MIS for NTC

The arrival time of the output signal Z for NTC transitions at the inputs is shown in Fig. 1. There are three curves, two corresponding to the SIS cases and one for the MIS case. It can be seen that the MIS effect occurs only when the Relative Signal Arrival Time (RSAT) between A and B is within a certain range, ($RSAT_{AB} = T_A - T_B$) which is bounded by the points LB and UB as shown in the figure. Thus the output arrival time is completely controlled by A when $RSAT_{AB} < LB$, after which the delay of A to Z is affected by signal B as well, and finally at $RSAT_{AB} >= UB$, B takes control completely. From the figure, the MIS effect on the delay from input A to output Z can be modeled as :

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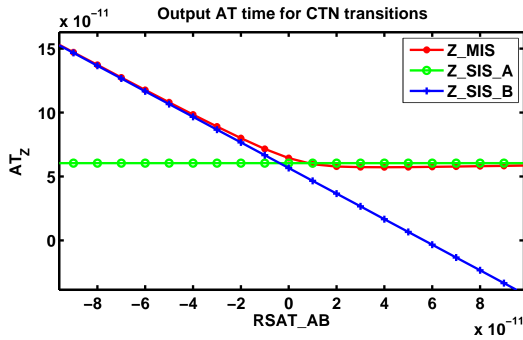
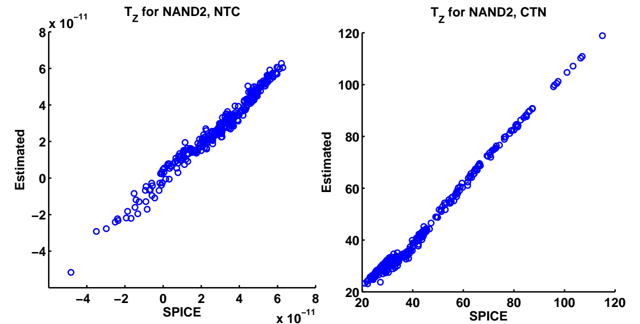


Fig. 2. MIS effect on A for CTN transition



(a) NTC transitions (b) CTN tranistions

Fig. 3. Estimate of AT_Z variable load, slope, RSAT

$$\Delta T_Z^{MA} = \begin{cases} 0 & RSAT_{AB} < -LB, \\ \frac{-\Delta T_Z^{SA}}{\Delta T_Z^{SB}+\Delta T_Z^{SA}}(RSAT_{AB}+\Delta T_Z^{SA})+c, & -LB <= RSAT_{AB} <= UB, \\ -RSAT_{AB}+\Delta T_Z^{SB}-\Delta T_Z^{SA}, & RSAT_{AB} > UB. \end{cases} \quad (1)$$

where $LB = \Delta T_Z^{SA}$, $UB = \Delta T_Z^{SB}$ and c is a fitting parameter that can be determined empirically. Typically, timing libraries contain pin-to-pin SIS delays of any gate characterized at different load-slope points. Since our model only requires knowledge of the SIS delay values, the dependency on load and slope is effectively captured. It was observed that the best fitting c has a weak relation with the load and slope values, but to minimize characterization effort, a single optimal value can be used without significant accuracy degradation. It can be seen that the gate delay in the MIS case is almost 50% smaller than the SIS case. To show that the model is robust over a range of input slopes and output loads, a Monte Carlo simulation was done where the output load and the signal slopes were drawn from a random sample. Input A is assumed to arrive at time $t = 0$ and the AT of input B has a normal distribution with mean 0 and $\sigma = 33ps$. The same value of the fitting constant c was used for each point. For each data point, the output AT is estimated using the MIS model presented above, and the scatter plot of the estimated values compared to those measured from SPICE is shown in Fig. 3(a). The maximum estimation error was $8ps$ which was 17% of the SIS propagation delay. If the output AT is estimated using just the SIS delays of the earlier arriving signals without accounting for the MIS effect, then the error in estimating the output AT is found to be 61%. Thus, accounting for MIS reduces delay estimation error by 44%.

B. MIS for CTN

A similar analysis was done for CTN transitions at the inputs and the corresponding output arrival times are shown in Fig. 2. For the CTN case, the transition is being propagated through the series network and hence the latest arriving signal determines the output arrival time. The MIS analysis for CTN transitions requires more characterization effort since the position of the input in the series stack also matters. In general, for the input closest to the output, the SIS delay is smaller than the MIS delay since all the intermediate nodes will be already discharged if all the other transistors in the series path are ON. For an input away from the output node, the SIS delay is larger than the MIS case, since it will have to discharge all the intermediate caps which have been charged up. Fig. 2 shows the same three curves for output AT with CTN transitions at the inputs. It can be seen that for CTN, the MIS region, (i.e. where both A and B together determine the output AT), is very small and the MIS curve does not deviate much from the SIS cases. For obtaining a smooth transition between the two asymptotes, we can approximate the MIS delay effect on input A as :

$$\Delta T_Z^{MA} = \frac{1}{k} log(\mathrm{e}^{(k(\Delta T_Z^{SA}+d_A))} + \mathrm{e}^{(k(\Delta T_Z^{SB}-RSAT_{AB}+d_B))}) - \Delta T_Z^{SA} \quad (2)$$

where k, d_A and d_B are fitting parameters that can be determined empirically similar to the NTC case. A similar expression was used to define the *soft-max* function in [7]. A Monte Carlo simulation was done with input signal slopes, output loads and RSAT values generated randomly, and the output AT of a NAND gate is measured when both inputs have CTN transitions. The same values of fitting parameters k, d_A and d_B are used for all the data points. The scatter plot shown in Fig. 3(b) compares the estimated values with those from SPICE measurements and it can be seen that the model is robust for a range of load and slope values. It can be seen that for CTN transitions, the SIS delay can either be an overestimate (negative MIS error) or an underestimate (positive MIS error) of gate delay depending on the RSAT values. For inputs closer to the output node, the MIS effect will tend to increase the delay, while for inputs away from the output, the MIS effect will decrease the delay. It was also observed that the MIS error for inputs farther from the output node tends to be very small, and the MIS error is significant only for inputs closer to the output nodes.

III. MIS FOR MULTI-INPUT GATES

As the number of inputs pins of a gate increase, the MIS error also increases. Fig. 4 shows the maximum percentage error in propagation delay caused by MIS noise for both CTN and NTC transitions, as the number of gate inputs is increased.

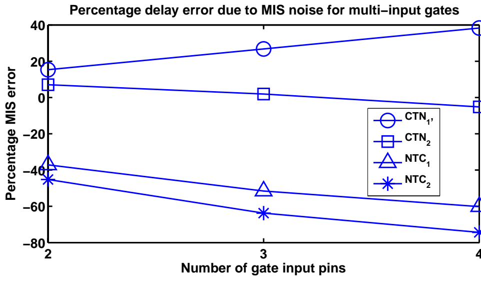
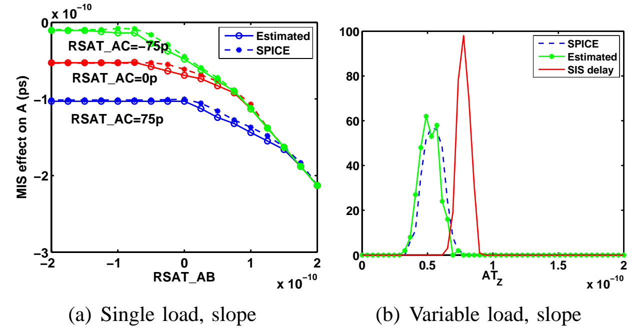


Fig. 4. MIS effect for multi-input gates



(a) Single load, slope (b) Variable load, slope

Fig. 5. MIS model for 3-input NAND gate, NTC

For each point, the MIS delay was measured for $RSAT = 0$, i.e., when all the inputs arrive at the same time. Thus the values plotted represent the maximum MIS error for each case. For CTN transitions, the number of transistors in a series stack increases with the number of input pins. In Fig. 4, CTN_1 shows the MIS error for the input that is closest to the output node, while CTN_2 is for the input farthest from the output node. Two similar curves, NTC_1 and NTC_2, are shown for NTC transitions at the inputs. It can be seen that for CTN transitions at the inputs, the MIS error is significant only when the input pin is closer to the output node and the error can be as high as 40%. For the input pin away from the output node, the MIS errors are negligible ($< 10\%$). For NTC transitions however, since multiple input signals mean multiple parallel current paths, the percentage delay errors due to MIS are very high starting from -45% for a 2-input gate and up to 75% for a 4-input gate. In this section, a model for the MIS error for NTC transitions is derived for a 3-input gate and the model can be easily extended to gates with more pins.

A. NTC transitions for NAND3

Consider a 3-input NAND gate, with NTC transitions on all the three inputs and input A arriving the earliest at time $t = 0$. The later arriving signals B and C, will affect the propagation delay of the gate due to the MIS effect. Let us assume that sequence of input arrival is A, B, C, i.e., signal A arrives the earliest followed by B and then C. Only the positive range of $RSAT_{BA}$ and $RSAT_{CA}$ therefore needs to be considered. If $RSAT_{CA}$ is large, then C does not have any influence and the MIS curve is similar to that of a 2-input NAND gate, but as input C arrives closer to A, the MIS curve changes. If we consider the MIS curve between the first two inputs only, then let s be the rate at which the output AT drops with $RSAT_{BA}$ (i.e., the slope), and the MIS error at $RSAT_{BA} = 0$ be given by m (i.e. the y-intercept). To estimate the MIS effect of input C, we need to determine how m varies with $RSAT_{CB}$. Once m is known, the slope of the new curve can be easily determined. We define a generic function $F(x, xp, yp, s)$ as follows:

$$F(.) = \begin{cases} s(x - xp) + yp + \epsilon, & \text{for } 0 <= x <= xp \\ yp, & \text{for } x > xp \end{cases}$$

Where ϵ is an empirical fitting constant. Thus $F(.)$ remains constant at yp for $x > xp$ and drops at the rate of s for $x <= xp$. This generic function can be used to describe the MIS curve, i.e. the output AT remains constant at $\Delta T_Z^{S_A}$ while $RSAT_{BA} > \Delta T_Z^{S_A}$. For $RSAT_{BA} < \Delta T_Z^{S_A}$, the value drops at the rate of $\Delta T_Z^{S_A}/(\Delta T_Z^{S_A} + \Delta T_Z^{S_B})$. It was observed that the variation in m with respect to $RSAT_{CA}$ also follows a behavior similar to $F(.)$. The value of m remains steady while $RSAT_{CA} > \Delta T_Z^{S_C}$. For $RSAT_{CA} < \Delta T_Z^{S_C}$, the value drops at the rate of $0.5 \times \Delta T_Z^{S_A}/(\Delta T_Z^{S_A} + \Delta T_Z^{S_C})$. This shows that the input B which is closest to A has the most impact on the output AT, while input C which arrives after B has a second order impact, in that it changes the rate at which output AT varies with $RSAT_{BA}$. The same trend can be continued for higher input gates, while taking into consideration the trade off between accuracy and effort. The complete method for estimating the MIS delay error for NTC transitions in a 3-input gate is shown below

$$T_Z^{M\prime} = F(RSAT_{BA}, \Delta T_Z^{S_A}, \Delta T_Z^{S_A}, \frac{\Delta T_Z^{S_A}}{(\Delta T_Z^{S_A} + \Delta T_Z^{S_B})}) \tag{3}$$

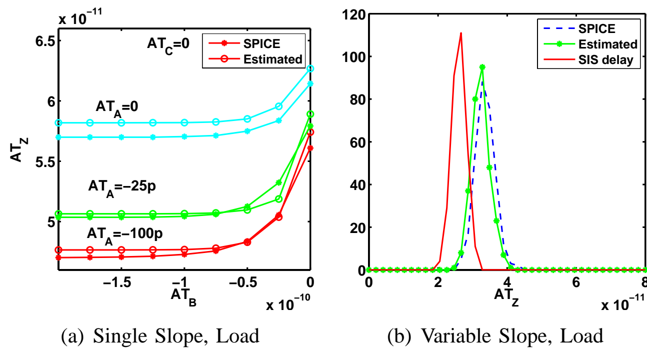
$$m' = T_Z^{M\prime}(RSAT_{BA} = 0) \tag{4}$$

$$m = F(RSAT_{CA}, \Delta T_Z^{S_C}, m', \frac{\Delta T_Z^{S_A}}{2 \times (\Delta T_Z^{S_A} + \Delta T_Z^{S_C})}) \tag{5}$$

$$s = (\Delta T_Z^{S_A} - m)/\Delta T_Z^{S_A} \tag{6}$$

$$\Delta T_Z^M = F(RSAT_{BA}, \Delta T_Z^{S_A}, \Delta T_Z^{S_A}, s) \tag{7}$$

where, $T_Z^{M\prime}$ and m' are intermediate variables. The output AT estimated using the above method is shown in comparison with values measured from SPICE simulations in Fig. 5. Three curves are shown for three different values of $RSAT_{CA}$, and it can be seen that the model estimates the MIS errors with reasonable accuracy. The only empirical constant here is ϵ, which has a weak dependency on input slope and output load, but a single optimal value can be used without loss of much accuracy. This can be seen from the plot shown in Fig. 5(b), which shows delay distribution of the timing arc from input A to output Z for NTC transitions at all three inputs. Monte Carlo simulations were done with input A arriving at $t = 0$, input signal slopes and the output loads are drawn from a Gaussian distribution. Arrival times of signal B and C are also assumed



(a) Single Slope, Load (b) Variable Slope, Load

Fig. 6. MIS model for 3-input NAND gate, CTN

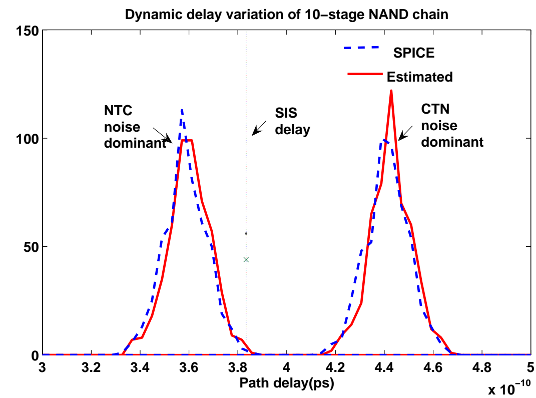


Fig. 7. Dynamic variation in path delay

to be Gaussian ($AT_B = N(30p, 16p), AT_C = N(50p, 16p)$). The SIS delay represents the distribution estimated when MIS effect is ignored. The maximum error in estimating the output AT using the above model was 15%, while the error in delay estimation is 51% if only SIS delays are considered. Thus accounting for the MIS effect reduces error by 35%.

B. CTN transitions for NAND3

As mentioned earlier, the MIS error for CTN transitions is negligible for inputs away from the output node and becomes significant only for inputs closer to the output node. For the following discussion, we therefore only consider the input pin closest to the output node, which in this case is input C. For CTN transitions, since the latest signal determines the output AT, let the sequence of input arrivals be A, B, C, i.e. C arrives the latest, and A and B affect the output AT due to the MIS effect. Both B and A will introduce MIS noise and hence affect the output AT. It was found that for CTN transitions, the total MIS error can be estimated by taking a scaled summation of the individual MIS errors as follows:

$$\Delta T_Z^{M_C} = \Delta T_Z^{M_{CB}} + 0.5 \times \Delta T_Z^{M_{CA}} \quad (8)$$

Where $\Delta T_Z^{M_{CB}}$ and $\Delta T_Z^{M_{CA}}$ are the MIS effect on input C due to inputs B and A respectively, and can by computed from 2. Output AT of a NAND3 gate estimated using the above model is compared with that measured from SPICE simulation in Fig.6(a). The graph shows the MIS error with respect to $RSAT_{BA}$ for three different values of $RSAT_{CA}$. The estimated values follow the SPICE curves with reasonable accuracy. Fig. 6(b) shows the results of Monte Carlo simulation for estimating the delay distribution of the timing arc from input C to output Z. The input slopes and output loads were obtained from a Gaussian distribution; similarly the ATs of signals A and B were treated as random variables, with $AT_A = N(-20p, 7p)$, and $AT_B = N(-30p, 10p)$. Signal C is assumed to arrive at $t = 0$. The maximum error in estimation using the above model is 16%, while the maximum error if only SIS delays are used was found to be 57%.

IV. Results and Conclusion

The MIS noise introduced due to variable side input arrival times is an important source of dynamic variation in path delays. Since side input signal arrival times are variable due to different logic paths and also due to process variations, $RSAT$ needs to be treated as a random variable. Fig. 7 shows the path delay variation of a 10-stage NAND chain. The dotted line in the center is the path delay when all off-path inputs are stable and non-controlling. In the other two cases, the off-path signal ATs were sampled from random distributions, and each off-path and on-path signal pair switches in the same direction (CTN or NTC). In both cases, we performed Monte-Carlo simulation using our proposed model and the estimated path delays can be seen to match those measured from SPICE very well. Thus our model can be used to make accurate estimates of path delay efficiently without having to do SPICE simulations.

In this paper, we have presented simple analytical models for estimating the delay effect due to multiple input switching. The model derived here can be used for efficiently and accurately estimating the dynamic path delay variation due to variable off-path signal arrival times. The advantage of the proposed analytical model is that it is based on already known data from the timing library, i.e. the SIS delays. Minimum characterization is required for the fitting constants and the model was found to be robust over a range of load and slope points.

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