Abstract – Due to aggressive scaling of device feature size to improve circuit performance in the sub-wavelength lithography regime, both diffusion and poly gate shapes are no longer rectilinear. Diffusion rounding occurs most notably where the diffusion shapes are not perfectly rectangular, including common L and T-shaped diffusion layouts to connect to power rails. This paper investigates the impact of the non-rectilinear shape of diffusion (i.e., sloped diffusion or diffusion rounding) on circuit performance (delay and leakage). Simple weighting function models for $I_{on}$ and $I_{off}$ to account for the diffusion rounding effects are proposed, and compared with TCAD simulation. Our experiments show that diffusion rounding has an asymmetric characteristic for $I_{off}$ due to the differing significance of source/drain junctions on device threshold voltage. Therefore, we can model $I_{on}$ and $I_{off}$ as a function of slope angle and direction. The proposed models match well with TCAD simulation results, with less than 2% and 6% error in $I_{on}$ and $I_{off}$, respectively.

I. Introduction

In modern CMOS technologies, minimum-sized devices are commonplace – particularly in low-power designs. In such gates, transistor width is only a few times larger than the minimum feature size and hence an understanding of gate width variation is important for accurate modeling of device characteristics (namely, delay and power). With the use of various resolution enhancement techniques (RETs) and design for manufacturability (DFM) methodologies, sub-wavelength lithography remains possible below the 65nm technology node [1]. However, new manufacturing problems due to the imperfect printing of gate length and width affecting parametric yield have become a major issue in post-lithography analysis [2],[3]. Many works have investigated the non-rectilinear poly gate shape and sought to model performance ($I_{on}$ and $I_{off}$) to account for the irregularity of the poly gate [4]-[10]. Most of these works slice non-rectilinear gates along the device width at a certain level of granularity, followed by a summation of $I_{on}$ (or $I_{off}$) of each slice to model $I_{on}$ (or $I_{off}$) of the non-rectilinear devices. More recent work has been proposed to include the edge effect in post-lithography simulation with the STI process [5],[17].

References [11],[12],[13] discuss edge effects, which are manifested as an unequal distribution of drive and leakage current densities across the width of the channel. In the Berkeley Short-Channel IGFET Model (BSIM) [14], this effect is modeled using the narrow-width component of the threshold voltage model [13]. The observation that the threshold voltage of modern MOSFETs is much lower near the edges than the center of the channel is central to the method proposed in this paper. With edge effects, we observe inverse narrow width effect (i.e., $V_{th}$ decreases as channel width decreases).

Most previous work assumes that the diffusion shape under the poly gate region is perfectly rectangular. However the diffusion shape is not actually rectilinear, because L and T-shaped diffusion regions often lead to a rounded diffusion under the poly gate. Figure 1 shows the lithography simulation contour of poly and diffusion in a 90nm standard cell using Calibre [15]. As can be seen from the figure, diffusion rounding happens in various locations with different forms.

In the sub-wavelength lithography regime, both gate width variation and diffusion rounding should be included in device analysis and characterization for accurate device modeling. Diffusion rounding is defined as occurring when source and drain diffusion areas do not form a perfect rectilinear shape under the poly gate region due to a 2D diffusion layout. These
bent diffusion layouts in L or T shapes often exist to connect source or drain to power supply (VDD or VSS) as shown in Figure 1. The extent of diffusion rounding mainly depends on the minimum distance from gate poly to the bent diffusion region. In 90nm and below, the minimum distance is about half of the minimum gate length. Thus the diffusion rounding size under the gate region is not negligible and we now see several 10s of nm of rounding in 90nm technology based on technology CAD (TCAD) simulation [15].

In this paper, we investigate the impact of diffusion rounding on device performance using a 3D TCAD simulator [16]. Simple weighting function models for both $I_{on}$ and $I_{off}$ are proposed to include this effect in post-lithography analysis. The rest of the paper is organized as follows. The 3D TCAD simulation setup for investigation of diffusion rounding effects is explained in detail in Section II. Section III describes how to calculate and verify weighted $I_{on}$ and $I_{off}$ models that can capture this effect. Section IV discusses results of diffusion rounding on a typical D flip-flop cell from a 90nm library in terms of leakage and delay. Section V concludes the paper.

II. TCAD Simulation of Diffusion Rounding

To understand the impact of diffusion rounding on device performance in terms of delay and leakage, we employ a 3D TCAD simulator [16] to generate the diffusion rounding shapes, and then measure $I_{on}$ and $I_{off}$.

Figure 2(a) shows two test patterns for diffusion rounding analysis in TCAD simulation; one includes diffusion rounding on the source side (left) and the other on the drain side (right). The extent of diffusion rounding mainly depends on the minimum distance from gate poly to the bent diffusion region. In 90nm and below, the minimum distance is about half of the minimum gate length. Thus the diffusion rounding size under the gate region is not negligible and we now see several 10s of nm of rounding in 90nm technology based on technology CAD (TCAD) simulation.

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side (right). Both 3D and top views of TCAD profiles with 40nm diffusion rounding are shown in Figure 2(b). We use nominal NMOS and PMOS devices with effective length 70nm and width of 400nm. Slope size, $w'$, is swept from 5nm to 40nm. TCAD model parameters used to generate the test device are shown in Table 1. TCAD simulation results are shown in Table 2 for the two test patterns. Results of “20nm both” and “40nm both” cases in which both source and drain side increase by 20nm and 40nm respectively are shown for comparison. As can be seen from the table, there are small changes in $I_{on}$ both for source-side and drain-side diffusion rounding. However, it is interesting to see that $I_{off}$ results are rather asymmetric; $I_{off}$ decreases due to source-side diffusion rounding (which is the common case in actual layouts) up to 20% in NMOS (17% in PMOS). On the other hand, for drain-side diffusion rounding $I_{off}$ increases then saturates as slope size increases.

The impact of diffusion rounding on $I_{on}$ can be explained by effective gate area change without any dependency on the rounded diffusion direction. For $I_{off}$, the leakage current reduction by source-side diffusion rounding is justified because in that case the rounded diffusion increases the effective device width (at source side) and slightly reduces the narrow-width effect (i.e., increases $V_{th}$ of the device) [13],[17]. The increased $V_{th}$ at the edge will reduce the leakage current exponentially. Therefore, we see smaller leakage than nominal due to source-side diffusion rounding. The narrow-width effect and corresponding $V_{th}$ change are only relevant for source-side rounding since $V_{th}$ is defined at the source rather than the drain. In summary, both $I_{on}$ and $I_{off}$ variations by the diffusion rounding can be explained by its size ($w'$) and location (source or drain).

Another factor contributing to this phenomenon is that VDD is applied at the drain; therefore source-side diffusion rounding decreases E-field at the source junction by increasing the effective channel length. On the other hand, drain-side diffusion rounding does not increase the effective channel length anywhere along the source junction. Total current density and E-field plots along the device width of nominal, nominal+20nm, and the two test patterns of slope size ($w'$) 20nm are shown in Figure 3 (a) and (b) respectively. As can be seen from the figures, diffusion rounding at source-side (red line) presents smaller current density and E-field at the device edge thus we expect smaller edge effect. 20nm drain-side diffusion rounding (blue line) shows current density and E-field values similar to the nominal device (black line). Again, these results indicate reduced $I_{off}$ by source-side diffusion rounding and small change in $I_{off}$ by drain-side diffusion rounded devices from a nominal device.
As explained in the previous section, the impact of diffusion rounding on device saturation current \( I_{on} \) can be explained by an effective gate area change without consideration of location dependency. Thus, the effect of diffusion rounding on \( I_{on} \) can be modeled as

\[
I_{on} = I_{on\_nom} \times \left(1 + \frac{w'}{W}\right)
\]

Here \( I_{on\_nom} \) is the on-current of the nominal rectangular device and \( w' \) is the height of diffusion rounding. \( W \) is the width of the nominal device (i.e., \( W_{\text{drawn}} \)). In reality, diffusion rounding is not strictly a straight line. However, we make this approximation as shown in Figure 2(a).

On the other hand, leakage current exhibits a location dependency. There is only a small change due to drain-side diffusion rounding while source-side diffusion rounding reduces leakage by a more significant factor. We focus on modeling \( I_{off} \) for source-side rounding since most layouts show primarily source-side diffusion rounding to connect to power lines (VDD and VSS) and to share the source. We model \( I_{off} \) due to source-side diffusion rounding as an exponential function of effective channel length at the edge:

\[
I_{off} = I_{off\_nom} \times K_1 \times \exp\left(\frac{L_{\text{nom}}}{L'}\right)
\]

Here \( I_{off\_nom} \) is the off current of the nominal rectangular device, \( K_1 \) is a fitting parameter (0.33 for NMOS and 0.34 for PMOS in this analysis), \( L_{\text{nom}} \) is nominal channel length, and \( L' \) is the effective channel length at the edge of diffusion rounding. \( L' \) can be calculated from the square root of \( \left(W^2 + L_{\text{nom}}^2\right) \). The fitting parameter \( K_1 \) is constant for a technology. For different technology nodes, this parameter is empirically fit to observed data.

Figure 4 shows the accuracy of the proposed models for different slope sizes from 10nm to 40nm. As can be seen, the proposed models capture the effect of diffusion rounding well in both \( I_{on} \) and \( I_{off} \) across different slope sizes.
To verify the proposed models with actual device lithography contours, we perform lithography simulations on six common device patterns that form different diffusion rounding shapes under the gate area. We then generate device structures based on these contours in TCAD simulations to measure $I_{\text{on}}$ and $I_{\text{off}}$.

Figure 5 shows the lithography contours for the six test inverter patterns. Empty solid lines are for drawn poly and diffusion and filled contours are for simulated poly and diffusion obtained using Calibre Workbench [15]. In this study we only generate NMOS devices (bottom devices) with the TCAD simulator. Devices 1, 3, 4, 5, 6 have diffusion rounding at either the top edge or bottom edge while Device 2 exhibits diffusion rounding at both edges. In these test patterns, the slope size varies from 11nm (Device 4) to 20nm (Device 2). Table 3 presents the $I_{\text{on}}$ and $I_{\text{off}}$ simulation results for the nominal drawn poly/diffusion and litho-contour based poly/diffusion. As shown in the contour2nom column, $I_{\text{on}}$ changes by up to 7% and $I_{\text{off}}$ differs by up to 40% (Device 2) due to diffusion rounding. The proposed models accurately capture $I_{\text{on}}$ and $I_{\text{off}}$ with diffusion rounding, with less than 2% and 6% error in $I_{\text{on}}$ and $I_{\text{off}}$, respectively (model2contour column). In Device 1, the model for $I_{\text{on}}$ overestimates the diffusion rounding impact because the proposed model cannot capture the poly flaring effects occurring in that device. In Devices 4 and 6, the model for $I_{\text{off}}$ underestimates the diffusion rounding impact because the model ignores the line edge roughness (LER) effects along the width. The remaining errors likely arise from the rectangular approximation of diffusion rounding geometry in the proposed models.

<table>
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V. Conclusions and Future Work

We investigate the impact of the non-rectilinear shape of diffusion on device on- and off-currents. We observe that diffusion rounding on the source side leads to a fairly appreciable reduction in subthreshold currents, while at the same time providing a small boost in on-current. We propose simple models to capture the diffusion rounding effects in post-lithography analysis. The test patterns studied, taken from a 90nm library, show that neglecting diffusion rounding can lead to 7% (40%) error in predicting $I_{\text{on}}$ ($I_{\text{off}}$). The proposed models show good match to simulation results and are within 2% in $I_{\text{on}}$ and 6% in $I_{\text{off}}$. A layout analysis of a commonly used sequential cell shows that diffusion rounding potentially reduces leakage, CLK→Q delay, and setup time. In our analysis we assume that there is no line edge roughness effect or poly flaring at the edge of the gate. Combining LER with diffusion rounding to create general models that account for various types of device shape irregularities is worthy of further investigation.

References


