Design Rule Optimization of Regular layout for Leakage Reduction in Nanoscale Design

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Abstract – The effect of non-rectilinear gate (NRG) due to sub-wavelength lithograph dramatically increases the leakage current by more than 15X. To mitigate this penalty, we have developed a systematic procedure to optimize key layout parameters in regular layout with minimum area and speed overhead. As demonstrated in 65nm technology, the optimization of regular layout achieves more than 70% reduction in leakage under NRG, with area penalty of ~10% and marginal impact on circuit speed and active power.

I Introduction

Leakage has become one of the predominant inhibitor to device scaling following Moor's Law. The manufacturing process is constrained by sub-wavelength lithography, as the Critical Dimensions (CD) are getting smaller than the optical wave length. Thus the impact of process variations on CD are getting significant with each technology scaling. Due to lithography process, the gate length of the device is distorted at the gate edge and the end of the gate which is referred to as non-rectilinear gate (NRG), as illustrated in Fig.1a. The NRG may increase sub-threshold leakage by more than 15X from that of an ideal layout [1] as illustrated in Fig. 1b for 65nm technology node. The shortening of poly line end may even cause device failure. To handle this manufacturing issue and improve design predictability, Regular Layout that follows single pitch and single orientation concept is recently introduced. By limiting the layout to regular pattern, Restrictive Design Rule (RDR) effectively enhances yield and minimizes the variations of gate length, particularly due to distortion caused by lithography.

Many studies have explored RDR-based layout prior to 65nm technology node and evaluated the impact on power, performance, area and yield due to RDR. In [5,6], RDR layout and its impact on lithography and yield have been analyzed. Other studies have discussed the trend of leakage due to technology scaling and process variations. Manufacturing aware physical design has been analyzed [7]. The Poly Pitch (PP), Poly End Extension (PEX), Contact Width (CW) and poly contact overlap are recognized as critical parameters that affect manufacturability of standard cells at 65nm technology node [8] and layout restriction to Poly Space (PS) significantly improves manufacturability even under process variations [8]. However, the important effect of NRG has not been incorporated. As the interaction between the layout and the leakage becomes more pronounced, there is a growing demand to optimize the layout under RDR for low power design.

In this paper, we investigate the optimization of regular layout, for the purpose to minimize the leakage due to NRG.. The key components in this procedure include: (1) the definition and projection of restrictive design rules; (2) physics based lithography simulation to predict NRG; (3) analytical transistor modeling for NRG; (4) circuit performance evaluation. The new optimization framework integrates manufacturability, device modeling, layout, and circuit performance in the early stage definition of design rules. By applying this method to several benchmark circuits at the 65nm node using Calibre workbench for aerial image simulation, we observe that as much as 70% reduction in the leakage can be achieved through the optimization of regular design rules, with area penalty of 10% and marginal overhead to circuit speed and active power. With the aggressive scaling of the minimum feature size, the optimal definition of RDR will play an even more critical role for better design predictability, lower leakage power, and higher design productivity.

This paper is organized as follows. The explored design rules and experimental setup are discussed in Section II. The layout optimization is performed at the 65nm node for several representative standard cells, since the standard cell

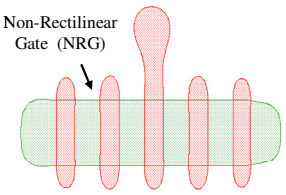

Fig. 1a. Post lithography aerial image of poly gate and diffusion showing NRG and line end shortening.

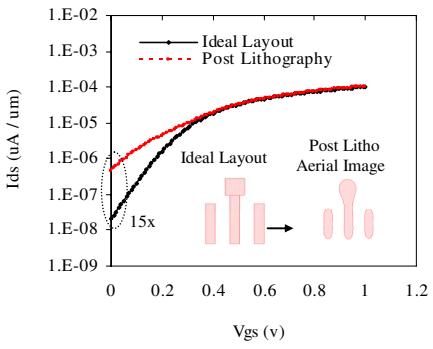

Fig. 1b. Leakage current fluctuation with ideal layout versus post litho, NRG leakage Model [1].

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library is one of the fundamental building blocks in today's VLSI design. The proposed procedure to optimize regular layout is discussed in Section III. It covers primary layout parameters, including Poly Space (PS), Poly Pitch (PP), Contact Width (CW), Poly to Diffusion Contact Space (PDC-S), as well as other parameters that affect cell area such as active width (W_p, W_n), Active Extension of poly (AEX) and Poly End Extension (PEX). These layout parameters are optimized to reduce the leakage due to NRG with minimum area and performance penalty. The optimization results are also analyzed in Section III.

II Experimental Setup and Model development

This section discusses the simulation setup and optimization methods that are applied in this study. The design rule constraints and layout choices are also discussed in detail. The flow diagram for regular layout optimization procedure is illustrated in Fig. 2. Design rules are defined and implemented in the layout technology file for few selective critical layers. The layouts are implemented according to the design rule for a handful of benchmark standard cells. Design rule verification and parasitic extraction is performed which are simulated in spice simulator for power and performance analysis. There are two crucial steps involved for leakage measurements. First is the aerial image simulation which takes the drawn poly gate test structures from layout as input and extracts post-lithography NRG profile along with L_{min}, L_{max}, mean and sigma. Second is the equivalent gate length (L_{eff}) model for NRG, that takes the post-lithography profile and generates the L_{eff} that is needed by spice simulator accounting for post litho and etch effects. Leakage is simulated using NRG leakage model for the benchmark circuits using Predictive Technology Model (PTM) for 65nm process technology [3]. The active power and performance are also simulated using PTM for further

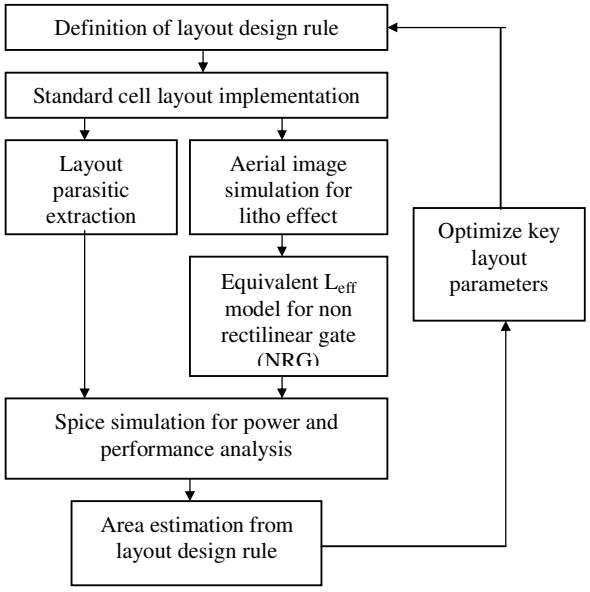

Fig. 2. Flow diagram for layout design rule optimization procedure.

Table 1: Design rule index and parameter range used for layout optimization.

Design Rule (nm)	Rule Index	Minimum value	Maximum value
Poly Pitch	PP	130	200
Poly Gate Length	L=(LW)	60	85
Poly Gate Width	W	325	650
Poly Space	PS=(LS)	65	195
Contact Width	CW	65	85
Poly End Cap	PEX	33	180
Poly to Diffusion Contact Space	PDC-S	60	130
Active Extension	AEX	65	260
Active Width Nmos	W_d=W_n	130	195
Active Width Pmos	W_d=W_p	195	260

where LW is Line Width = L and LS is Line Space=PS.

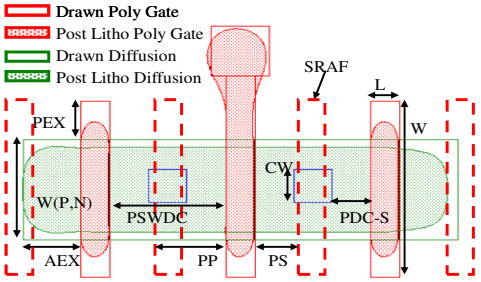

Fig. 3. Post litho aerial image super imposed on top of ideal layout illustrating rule index of identified design rule parameters used for optimization. sub-resolution assist feature (SRAF) used to overcome the limitation of off-axis illumination (OAI) pitch specific resolution enhancement.

analysis. Due to application of regular layout, it is completely valid to calculate the area from the drawn layout for various deign rule change for optimization purpose.

A. *Critical Design Rules*

The default layout design rule set have many entries that are scaled according to the lambda rules specified in the technology file for 65nm process node. Yet only some specific set of critical design rules are identified for optimization and are examined as required. The critical rule index along with minimum and maximum range of critical layout parameters used for optimization is illustrated in Table 1 and Fig. 3. The rule index specified in this table will be used for all further discussions. ITRS [4] projection for minimum poly pitch (ie. Half pitch = 65nm) is used as the starting point in setting up the minimum PP for experiments. The critical parameters in Table 1 are preferred for two reasons. These parameters either affect leakage, area or overall circuit performance such as manufacturability, active power and circuit speed. In general PP is expressed as:

$$PP = L + PS \quad (1)$$

The PS is the critical parameter that highly impact image printability during manufacturing process [8]. Thus minimum and maximum values of the PP is one of the key layout parameter used for optimization as it highly impacts leakage current fluctuation due to NRG. From (1), as L is fixed (ie. L=65), PS can be optimized such that the leakage due to NRG and area penalty due to RDR is optimal.

PDC-S also contributes to PS as it is expressed as:

$$PSWDC = CW + (2PDC\text{-}S) \quad (2)$$

Where PSWDC is Poly Space with Diffusion Contact.
In order to meet regular layout constraint, from (2), if CW is defined and set to optimal value, then PDC-S can be optimized such that it meets the criteria of PS in (1) with a sub-resolution assist feature (SRAF) in between two poly gates where the contact is placed as illustrated in Fig. 3. PEX combined with diffusion width (W_p, W_n) limits printability due to line end shortening introduced during lithography process and in turn impacts overall circuit performance. Also AEX impacts printability, thus contributes to post litho circuit performance and pre litho area impact for RDR optimization.

B. Benchmark Standard Cell Circuits

The layout implementation and design rule analysis are performed on few benchmark standard cells in the library. Three cells are identified for detailed analysis that includes NAND gate, XOR gate and one bit full Adder. By analyzing these basic cell, the design rule impact can be accurately estimated for the smallest, medium and largest cells of the standard cell library. The layout is implemented for three cases for the benchmark circuits: (1) using typical classical layout design style with random orientation for poly gate that can be manufactured but can not sustain process variation, (2) using typical regular layout style for comparison with our proposed approach where a typical regular layout is defined as the regular layout with very minimal area penalty compared to random layout. The PS in typical regular layout for a given process window will be smaller than that of the optimized PS. Thus there is less area penalty for this style but the leakage will be higher than the optimized layout due to significant gate length variations, and (3) optimized regular layout style according to our proposed layout optimization procedure in order to reduce leakage with optimal area penalty compared to typical regular layout.

Typical layout design rule for 65nm process technology is used in implementing the initial benchmark gates and the optimal design rules are derived using optimization procedure discussed in later section. For our low power layout design, minimum diffusion width for NMOS and PMOS for a unit inverter is defined as Wn=130nm and Wp=260nm. The W_p and W_n for each type of benchmark circuit for various design rule sets are kept constant across all optimization phase in order to have a fair comparison of performance and active power impact. The cell height range from 1.1u to 1.6u depending on the geometries chosen between minimum and maximum design rule parameters defined in Table 1. For illustration of concept, we use the classical random layout style and typical regular layout style of XOR gate shown in Fig. 4a and Fig. 4b. The random layout is called so, because the poly gate do not follow specific orientation in the layout. It can be placed vertically or horizontally according to the needs, thus save some area at the cost of manufacturing yield. Where as the so called regular layout follows single orientation [9], single pitch concept for poly gates and poly routing is not allowed. Metal-1 and Metal-2 are used for internal cell routing. The same approach is followed for the fore mentioned benchmark circuits.

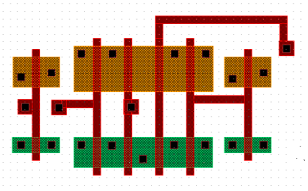

Fig. 4a. Random layout of the XOR gate showing gate, diffusion (Wp, Wn) and contacts.

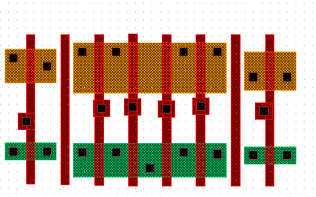

Fig. 4b. Regular layout of the XOR gate showing gate, diffusion (Wp, Wn) and contacts.

C. Post Lithography Aerial Image Simulation Model

Calibre workbench (calibrewb) along with calibrelv is used for aerial image simulation for lithography verification. TCCALC engine with scalar diffraction model is used along with model based Optical Proximity Correction (OPC) in the Calibrewb. Two major lithography simulation models are used by calibrewb in performing aerial image simulations that includes optical model and resist model. For optical model, the process window is calibrated for 65nm technology process assuming immersion lithography technique [10, 11, 12] with illumination wavelength λ=157nm, maximum theoretical limit of numerical Aperture NA=0.95 and refractive index of water n=1.437 for better printability at 65nm technology node. Off axis illumination (OAI) technique is applied as OAI amplifies certain pitch at the cost of others. This phenomena is called “Forbidden” pitch [13,14]. In order to overcome this OAI limitation, sub-resolution assist feature (SRAF) [5] is accounted in our optimization. Thus OAI combined with SRAF is added benefit to our approach as we intend to follow single pitch, single orientation concept for our layout style in order to alleviate the impact of post litho NRG in reducing leakage and improving overall circuit performance. Due to the regular layout style, it is completely valid to calibrate the optical model for selective pitch versus others with the help of SRAF. OAI factor of 0.5 is identified during process window calibration due to better printability even at defocus conditions. ITRS [4] specified resist thickness is expected to be < 225nm. For our process window calibration, resist thickness of 125nm is assumed for resist model.

The post litho NRG effect is studied using test layout structures specified in Fig. 3. Dummy poly gates are used in the place of SRAF. The poly and diffusion layers are analyzed using calibrelv lithography simulator. CD variations from this structure is used for analysis and optimization of PS with and without diffusion contact, PEX and AEX for various benchmark circuits. The CD variation (ie.) NRG of the gate L is studied by estimating post litho poly edge errors and line end shortening. To first order approximation, the post litho L_{min}, L_{max}, mean and sigma variation due to NRG and effective poly width (W_{eff}) is estimated for all gates in the test structure. Each

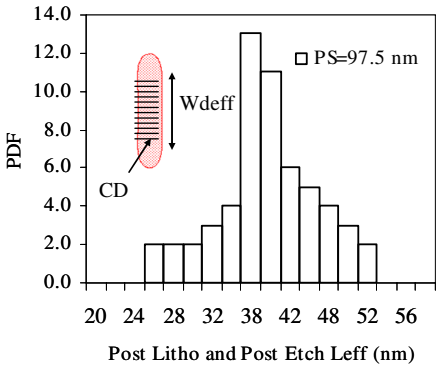

Fig. 5. Normalized PDF of post litho, post etch effective channel length (L_{eff}). CD measured along effective diffusion width (W_{deff}) for a simple test structure. L_{eff} = CD – etch effect. Etch effect is ~30nm for 65nm technology node.

sample slice of the poly gate is split into N segments of Wc width (Wc = ~5nm) along the W. The CD variation is calculated at 30% of the maximum image intensity for each sample segment [15]. The NRG profile obtained using this scheme are then applied as an input to L_{eff} NRG leakage model for leakage measurement. The PDF of L_{eff} obtained from post litho simulation with etch effect for any particular PS follows Gaussian distribution as illustrated in Fig. 5. The distribution is not exactly the same for different types of layout styles for various standard cells and mostly depending on the layout style and spacing between the CD for a specific process window.

D. Equivalent L_{eff} Model for NRG Leakage Analysis

The effective Gate voltage dependent Equivalent gate length (L_{eff}) model [1] is used for the prediction of actual off power due to NRG roughness introduced in gate profile for different types of layouts. Input data for this equivalent L_{eff} NRG model is the L_{min}, L_{max}, mean and sigma obtained from post litho aerial image simulations. By applying the equivalent gate length (L_e) concept, the NRG models has three components in deriving the equivalent L_{eff} [1]. The L_e^{min} is a function of L_{min} and sigma of all the lengths that form the gate section and is expressed as:

$$L_e^{\min} = L_{\min} + \ln(\sigma W / Wc) \quad (3)$$

Where as L_e^{max} is a function of mean gate length and sigma and is expressed as:

$$L_e^{\max} = \mu - \ln(\sigma) \quad (4)$$

And the L_{eff} is expressed as:

$$L_{eff} = L_e^{\min} + \frac{\Delta L\sqrt{\alpha} Vgs}{\sqrt{\alpha (Vgs)^2 + 1}} \quad (5)$$

Where $\Delta L = L_e^{\max} - L_e^{\min}$ and α is the fitting parameter for ΔL at 65nm. Leakage power is estimated by integrating the current sourced from supply when the standard cell is in standby mode. Spice simulation for various standard cell layouts show an exponential dependence of leakage power on L_e^{min}. The Leakage power is calculated by substituting model equation (5) for L_{eff} in place of gate length in spice simulations for PTM 65nm technology [3]. Verilog-A model for transistors are used in integrating equivalent L_{eff} model with spice in transient analysis.

III Optimization of Regular Layout

The optimization method used in identifying the RDR are discussed in this section. We use the one bit full Adder for our illustration in this section. Any optimal design rule parameter identified using this approach can be applied across the entire standard cell library. The optimization of regular layout is performed by analyzing each individual critical design rule parameter for the range specified in Table1. Each parameter is optimized individually and used as input for optimizing the next parameter.

A. Optimized Design Rule Variables

The priority of optimization is defined in the order specified: PS with and without CW, PEX, W, L and AEX. The critical parameter PS is swept from the minimum value to the maximum value specified in Table 1 and gate profile is obtained using aerial image simulation. Using equivalent L_{eff} model, NRG leakage is measured. The leakage (E_{off}) due to NRG is very sensitive to CD min obtained from the aerial image simulation[1]. Fig. 6 illustrates CD min sensitivity to PS, PEX and L. The layout area for various PS is estimated from the original regular layout. In case of poly space with diffusion contact (PSWDC), PDC-S is derived in such a way that it meets the criteria of un-contacted PS with a sub-resolution assist feature (SRAF) in between two poly gates where the contact is placed as illustrated in Fig. 3. The optimum PS is obtained such that the leakage impact and the area penalty due to RDR is optimal as shown in Fig. 7. For the calibrated process window, the optimal PS is ~97.5nm with 73% reduction in E_{off} and ~10% area penalty. Active energy (E_{active}) and circuit speed (T_{pd}) have marginal impact of ~12.5% due to PS optimization as illustrated in Fig. 8. Due to OAI it is observed that the benchmark circuits are too leaky beyond certain PS (~150nm) and so functional failure is observed. With a SRAF feature in between two contacted poly gate, PDC-S can be derived as:

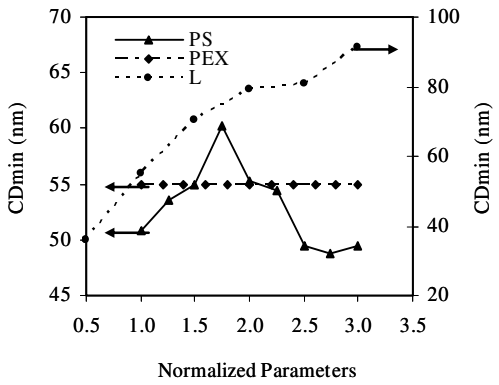

Fig. 6. CD min trend for PS, PEX and L optimization. CD min is affected profoundly by PS. Once the PS is optimized then the poly width (W) has no impact on CD min.

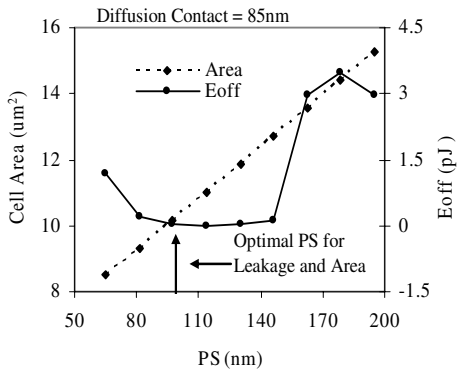

Fig 7. Finding optimal PS for leakage energy (E_{off}) and area for CW=85nm.

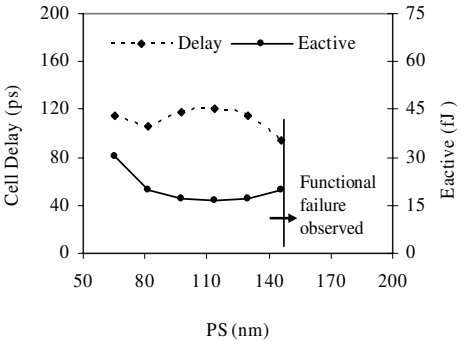

Fig. 8. Marginal impact to active energy (E_{active}) and speed (T_{pd}) due to PS. Due to OAI forbidden pitch, circuit failure observed beyond PS=150nm.

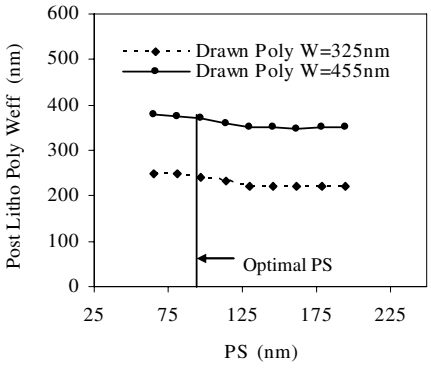

Fig 9. Post litho effective poly width (W_{eff}) has marginal impact with respect to PS.

$$[(2\ PS) + L - CW]/2 = 87.5nm \quad (6)$$

For the optimized PS, the CW of 85nm is assumed in (6) as there is sufficient space available for larger CW in between two poly gates with SRAF in place of contact. The optimized PS, PDC-S and CW are used for PEX optimization. From Fig. 6, it can be observed that once the PS is optimized the PEX does not have much impact to CD min. Thus PEX is heuristically set, so the maximum W_d can be printed without any yield impact as illustrated in Fig. 1a. From aerial image simulation it is observed that, PEX is required to be at least 1L. The W_d max range is ~260nm for our experiments. Thus accounting for process variations, PEX is fixed at *1.5L=97.5nm* and so the optimal poly width (W) is calculated as $W_d + 2PEX = 455nm$. Impact of post litho poly width (W_{eff}) due to PS is illustrated in Fig. 8. PS does not seem to impact W_{eff} and so the device yield is mostly dependent on PEX with respect to diffusion width (W_d). L optimization is performed using all previous optimized layout parameters. From Fig. 6, it is evident that for L below optimized LW=65nm, CD min is distorted more compared to L above the optimized LW. AEX is also considered in our optimization as it impacts the cell area as well as circuit speed. For contacted diffusion, AEX is mostly defined by the CW, PDC-S and active overlap of contact (X). Using all the optimized parameters and eliminating X for our first order approximation, AEX is calculated as: $CW + PDC\text{-}S + X = 172.5nm$. For single pitch single orientation design style, AEX with and without contacted diffusion can be kept same. Thus the yield requirement is met as illustrated in Fig. 1a without causing post lithography device failures.

B. Effect of Defocus on Optimized Layout

The impact of defocus on post litho NRG parameters (L_{min}, L_{max}, mean and sigma) for optimized layout is shown in Fig. 10. Since the NRG L_{eff} leakage model is sensitive to L_{min} from post litho simulations, variation in L_{min} is focused in detail. For a defocus of +/-15nm, approximately +6.8nm to -7.7nm variation in L_{min} is observed for the calibrated process window. The L_{min} for positive defocus range will reduce leakage and slow down the circuit speed due to increase in L_{min}, where as negative defocus range will increase the leakage as well as speed and could cause fatal failure due heavy leakage caused by reduction in L_{min}.

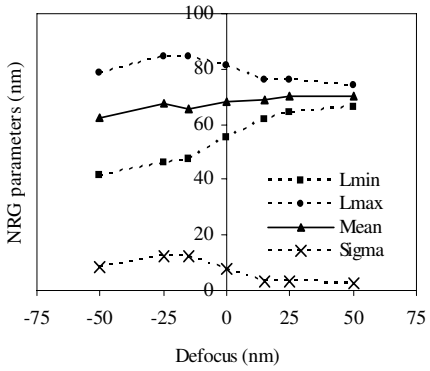

Fig. 10. Effect of defocus on post litho parameters needed by NRG L_{eff} model for optimized layout with PS=97.5nm and L=65nm.

C. Optimized Results

Comparative analysis of three benchmark circuits (NAND, XOR and one bit full Adder) are shown in Table 2. All the design metrics (T_{pd}, E_{active}, E_{off} and area) are compared for typical regular style layout and optimized regular layout (following our proposed layout optimization method). Optimized regular layout has 73% reduction in E_{off} for XOR and one bit full Adder with area penalty of

Table 2: Comparative analysis of regular layout design metrics (ie.) leakage, area, active power and performance for bench mark circuits with respect to typical regular layout style.

Layout Design Style	T_{pd} (ps)	E_{active} (fJ)	Area (um2)	E_{off} (fJ)
NAND				
Classical Random	30.18	1.227	1.142	0.0916
Typical Regular	33.58	1.316	1.187	0.0228
Optimized Regular	37.66	1.536	1.231	0.0146
Optimized vs Typical Regular (%)	12.15	16.72	3.71	-36.12
XOR				
Classical Random	90.44	11.04	3.900	411.0
Typical Regular	90.82	7.53	4.260	52.63
Optimized Regular	97.56	7.21	4.612	13.97
Optimized vs Typical Regular (%)	7.42	-4.20	8.26	-73.46
One bit full Adder				
Classical Random	110.80	30.52	8.480	1172.0
Typical Regular	104.00	19.56	9.341	184.5
Optimized Regular	117.00	17.25	10.173	50.15
Optimized vs Typical Regular (%)	12.50	-11.81	8.91	-72.82

~9%. The NAND gate also has a E_{off} improvement of only ~36% with area penalty of ~4%. Marginal impact of ~5 to 12.5% observed for E_{active} and T_{pd} for XOR and one bit full Adder.. Where as for the NAND gate, thought the percentage difference is ~12 to 17% for T_{pd} and E_{active}, the magnitude of change is ~4ps for T_{pd} and ~0.2fJ for E_{active}. Final optimized RDR parameters are shown in Table 3 according to discussion in Section III A.

The cell delay of the optimized regular layout is ~12.5% higher as compared to that of typical regular layout. This is due to the fact that the wire capacitance of the switching net in optimized layout is slightly higher. Careful optimization of metal width and an optimal choice of shared diffusion can help alleviate delay penalty during power optimization.

IV Summary and Conclusions

Due to manufacturing limits, leakage measurement based on ideal layout is not the sufficient metric for low power designs. Based on NRG L_{eff} leakage model, there is significant fluctuations to I_{off} between ideal layout and post litho NRG. From the regular layout optimization study, it is evident that the PS is the critical layout parameter that has significant impact on leakage and area due to NRG. We have shown that, with the help of regular layout optimization technique, E_{off} due to NRG is reduced by 73% for PS=97.5 nm with an area penalty of 9 % and marginal impact on E_{active} and T_{pd} of ~5 to 12.5% for one bit full Adder. Thus for low power designs, the proposed layout optimization method can be applied during design phase of the product cycle in defining RDR for regular layout that helps reduce leakage and improve product yield.

Acknowledgements

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Table 3: Final optimized parameters for regular layout. The typical values are scaled for λ=157nm from it original λ=193nm wavelength and corresponding settings [8] and used for comparative analysis.

Optimized Layout Parameter	Typical value (nm)	Optimized Value (nm)
PS	81	97.5
PDC-S	71	87.5
CW	80	85
PEX	65	97.5
W	455	455
L	65	65
AEX	151	172.5

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