Non-Gaussian Statistical Timing Models of Die-to-Die and Within-Die Parameter Variations for Full Chip Analysis

Katsumi HOMMA Izumi NITTA Toshiyuki SHIBUYA
FUJITSU LABORATORIES LTD. 4-1-1 Kamikodanaka, Nakahara-ku, Kawasaki-shi, 211-8588 Japan
E-mail: {km.homma, nitta.izumi, shibu }@jp.fujitsu.com

Abstract - Statistical Timing Analysis (SSTA) is a method that calculates circuit delay statistically with process parameter variations, die-to-die (D2D) and within-die (WID) variations. In this paper, we model that WID parameter variations are independent for each cell and line in a chip and D2D variations are governed by one variation on a chip. We propose a new method of computing a full chip delay distribution considering both D2D and WID parameter variations. Experimental results show that the proposed method is more accurate than previous methods on actual chip designs.

I Introduction

With the advent of deep sub-micron technologies, the delay variations caused by process, temperature, voltage drop and cross talk are increasing. Static timing analysis (STA) uses the worst-case corner variations in delay calculation, which means that it calculates the delay assuming that all of the process variations cause each gate to take the largest delay during set-up checking. However, since the random parts of the variations of each gate cannot be worst simultaneously on the same chip statistically, STA is usually optimistic by a large margin, which causes over-estimation in delay calculation, requires excessive delay margin in design phases, and makes the timing closure difficult.

Statistical static time analysis (SSTA) handles the random parts of the process variations as probability distributions to calculate the delay statistically. It has been studied over the years [1,2]. Several approaches to model the delay distribution have been proposed, and can be categorized in the following three classes:

1) Gaussian Approach [3,4,5,6]
Parameter variations are expressed either as a single normal random variable or a linear sum of normal variables. The delay distribution will be Gaussian. Statistical operations can be executed with less computational penalty, but this approach has a limitation in expressing the non-Gaussian on statistical maximum operations.

2) Non-Linear Gaussian Approach [7,8,9]
Parameter variations are expressed as a non-linear function of normal random variables. It can express any distributions other than Gaussian. However, the statistical maximum operation contains theoretical errors because it is not closed with respect to statistical operations, and it is time-consuming compared with the Gaussian approach.

3) Piecewise Linear Approach [10,11,12]
The distributions of parameter variations are expressed in a piecewise linear approximation. It can express any form of distributions, and provide accurate statistical operations if fine intervals are allowed. However, the computational time of the operations increases with the number of intervals.

On the other hand, in modeling the delay distribution, it is important to model die-to-die (D2D) parameter variations and within-die (WID) parameter variations separately [1,2]. D2D parameter variations result from lot-to-lot, wafer-to-wafer, and global variations within wafer, and give the same parameter variations to each gate on a chip. WID parameter variations result from random noises during fabrication, and can be divided into correlated or systematic parts and independent parts. D2D parameter variations are required to be considered in order to predict the accurate timing yield for the mass production processor designs which use bin sorting by speed.

In this paper, we adopt the delay model of [11] for D2D and WID parameter variations as follows:

$$D = D_{norm} + \Delta D_{inter} + \Delta D_{intra} \quad (1)$$

Where D_{norm} is nominal delay, ΔD_{inter} is delay variation due to D2D parameter variation and ΔD_{intra} is delay variation due to WID parameter variation. D2D and WID parameter variations are independent. We call D as total delay and distribution of D as total delay distribution. Total delay distribution can be obtained as statistical ADD (see Section 2.3) of D2D and WID parameter distributions. We adopt the piecewise linear approach to model the delay distribution of WID parameter variations, which can handle the non-normality of the delay distributions caused by statistical operations and the non-normality of gates and wires [9].

An approximate calculation method for statistical maximum operations to consider the D2D and WID parameter variations based on piecewise linear approach was proposed in [11]. It works fine for a small number of paths, but the calculation errors become large as the number of paths increases.

To calculate the statistical maximum operations accurately, we introduce new non-Gaussian model for D2D parameter variations. The idea is as follows:

For given two paths, the statistical maximum of their WID parameter variations can be obtained with the multiplication of CDFs (Cumulative Distribution Function) of their WID parameter variations. Then, we calculate the statistical maximum of the two paths considering the WID parameter variations and the correlations of their D2D parameter variations. This method is theoretically accurate, which will be discussed in detail in Section 3.1. Finally, the D2D parameter variations of the two paths will be obtained by moment matching applied to their WID variations and their statistical maximum. To handle more than two paths, we apply this iteratively. The obtained D2D and WID parameter variations are used to calculate the statistical maximum for the next path.

The main contributions of this paper are as follows:

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- We provide a new method to extract the statistical maximum of D2D parameter variations of the two paths from the statistical maximum of WID parameter variations and their statistical maximum considering both D2D and WID variations.
- A path pruning technique is proposed to speed up the method.
- We demonstrate the accuracy and efficiency of the proposed methods on three typical actual designs.

The rest of the paper is organized as follows. In Section II, we review the path analysis and the statistical delay calculation. In Section III, a statistical maximum operation method and a speed-up technique are proposed. Section IV shows the experimental results. Section V concludes this paper.

II. Preliminary

2.1 *Check Path, Check Path Delay and Chip Delay*

For given a pair of flip-flops, the whole set of the circuit elements and paths between the pair, ones on the shared clock path from the clock source and the pair is defined as a *check path*. Fig. 1 shows an example of a check path. S is the shared clock source of FF1 and FF2. The delay of the path from S to D of FF2 through FF1 is defined as D_{path}, and the delay of the path from S to CLK pin of FF2 as C_{path}.

We define a *check path delay* as follows:

Check Path Delay = $D_{path} - C_{path} - C$. (2)

where C is the circuit dependent constant time including the setup time of FF2. We can obtain the frequency of the check path from inverse of the check path delay. We define the maximum of all check path delays in a chip as the *chip delay*. We can obtain the frequency of the chip from inverse of the chip delay.

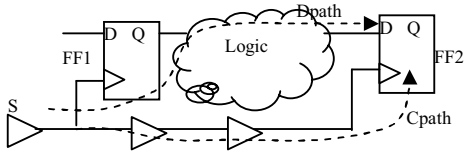

Fig.1. Check Path

2.2 *Check Path delay Distribution and Chip Delay Distribution*

When the delays of elements in a chip are distributed due to variations, the check path delay will be distributed, and is called *check path delay distribution*. Then, the chip delay will be distributed in the same way, and is called *chip delay distribution*. Timing yield can be calculated from the chip delay distribution.

For given D2D and WID parameter variations to each element of a chip, one method to calculate the chip delay distribution was proposed by [11]. It uses the following two steps:

Step 1: Calculation of D2D and WID check path delay distributions

For each check path in the chip, calculate the D2D and WID delay distribution of D_{path} separately. Likewise, calculate the D2D and WID of C_{path}. Then, calculate the check path delay distribution from equation (2).

Step 2: Calculation of chip delay distributions

Apply the statistical maximum operation over all D2D and WID of D_{path} and C_{path} to obtain the chip delay distribution.

In Step 2, Monte Carlo simulation would yield most accurate results. However, it is time-consuming, because for actual chip designs more than hundred thousands of check paths should be handled at a time for each simulation event. Also piecewise linear approach we adopted requires huge amount of memory to save the whole check path delay distribution.

One way to avoid this problem is to calculate the chip delay distribution *iteratively*. First, choose any two check paths from the set of all the check paths, and calculate their check path delay distribution. Then, choose another check path, and calculate its check path delay distribution and the check path delay distribution obtained from the previous calculation. Continue this process until all of the check paths are processed.

Two approximations are proposed by [11] to execute Step2. They are discussed in Section 2.5.

2.3 *Statistical ADD and MAX*

A directed acyclic graph G=(V,E) called *Timing Graph* is used to express signal flows of a circuit. Each node v_i represents input or output of a gate and the direction of an edge represents the direction of the signal in the circuit. Each edge has a weight, which is a random variable of gate or line delay variations. We show an example of timing graph in Fig.2. SSTA executes statistical operations from v_0, the source, to v_5, the target. Each node saves the result of the statistical operations as a delay random variable from v_0 to the node.

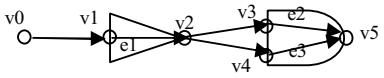

Fig.2 Timing Graph [15] ©IEICE 2007

Fundamental statistical operations of SSTA consist of statistical ADD and statistical MAX.

Statistical ADD will be applied to a node with a single input edge. For example, the random variable of v_2 can be calculated as statistical ADD of the random variable of v_1 and that of the edge e_1. Let X be the random variable of v_1, Y be the random variable of e_1 and Z be the random variable of v_2. Then Z = X+Y. If X and Y are independent, statistical ADD can be calculated as convolution of two random variables as follows.

$$F_z(t) = \int F_x(t-s) f_y(s) ds \quad (3)$$

Where F_z is CDF of the delay random variable of v_2, F_x is CDF of v_1 and f_y is PDF (Probability Density Function) of the random variable of e_1.

Statistical MAX will be applied to a node with multiple inputs. For example, v_5 has two inputs, e_2 and e_3; we calculate statistical MAX of the delay random variable of e_2 and e_3. Let X be the delay random variable of e_2 from the source, Y be that of e_3 from it, and Z be the delay random variable of v_5. Then Z = max(X,Y). In this case, it is difficult to calculate CDF or PDF of Z because the delay random variables, X and Y, which have the common edge e1 in the paths to the source, are not independent. If X and Y are independent, CDF of statistical MAX, Smax(X,Y), is calculated as follows.

$$Smax(x,y)(t) = F_x(t)F_y(t) \quad (4)$$

Where F_x is CDF of X and F_y is CDF of Y. The CDF calculated by (4) gives an upper bound of Smax(X,Y) [10], even if X and Y are not independent.

2.4 *Statistical Subtraction*

As shown in equation (2), the delay random variable of C_{path} should be subtracted from that of D_{path} to obtain that of check path delay statistically. *Statistical subtraction* can be calculated in the same manner as statistical ADD. Let X and Y be the delay random variables of D_{path} and C_{path}, respectively. If X and Y are independent, the delay random variable Z = X-Y is calculated as follows.

$$F_z(t) = \int F_x(t+s) f_y(s) ds \quad (5)$$

Where F_z is CDF of Z, F_x is CDF of X and f_y is PDF of Y.

2.5 *D2D and WID parameter Variations*

Equation (1) is the delay variation model that we adopt for our proposed method. Since we also adopt the piecewise linear approach to model the delay distribution of WID parameter variations, any shape of the distribution of WID parameter variations can be expressed. We assume WID parameter variations are independent for each gate or line. In general, WID parameter variations have correlation for each gate or line. Practically, since equation (1) can contain one correlated random variable, ΔD_{inter}, we can simply express the WID correlation with putting the correlated parts into the D2D parameter variations.

D2D parameter variations give variations uniformly to all elements of a chip. They are modeled by one delay random variable for a chip. To cope with non-Gaussian variations and to be closed with respect to statistical operations, we model D2D parameter variations as follows.

$$\Delta D_{inter} = ap*z \ (z>0), \quad an*z \ (z<0) \quad (6)$$

Here "ap" and "an" are *positive coefficient* and *negative coefficient,* respectively, those are given by cell libraries and technology parameters, and z is a random variable that is the same for all gates and lines. The mean of z is zero and its standard deviation is one. D2D parameter variations express the correlated parts of the total delay variations for all gates and lines in a chip.

According to the definition of statistical MAX, for given two parameter variations,

$d_1 = a_1*z \quad d_2 = a_2*z$,

it should be:

$\max(d_1,d_2)=\max(a_1,a_2)*z \ (z>0), \min(a_1,a_2)*z \ (z<0)$. This means that the simple variation model of $\Delta D_{inter} = a*z$ for all z cannot express this result of statistcal MAX any more. Generally, approximation methods, such as moment match, will be applied to obtain the resulatant parameter variation with errors. However, equation (6) is closed with respect to statistical MAX operations, which means that statistical MAX of the two parameter variations in equation (6) can be calculated rigorously in the same expression of equation (6).

For given two D2D parameter variations,

$d_1 = ap_1*z(z>0), an_1*z(z<0) \quad d_2 = ap_2*z(z>0), an_2*z(z<0)$,

statistical ADD can be expressed as

$$d_1+d_2 = (ap_1+ap_2)*z \ (z>0), \ (an_1+an_2)*z \ (z<0) \quad (7)$$

and statistical MAX can be done as

$$\max(d_1,d_2)=\max(ap_1,ap_2)*z \ (z>0), \ \min(an_1,an_2)*z(z<0). \quad (8)$$

Equation (7) and (8) show that equation (6) is closed with respect to statistical operations, ADD and MAX.

This delay variation model is simple. However, practically, we could predict timing yield for microprocessor designs successfully with fitting the random variables to the delay results of ring oscillators [13].

Algorithm: Iterative Chip Delay Distribution Calc.
Input:F1,F2,F3,…,FN: check path delay distribution
Output:D:chip delay distributions
1. D = Smax(F1,F2) 2. For i = 3, …, N 3. D = Smax(D, Fi)

Fig. 3. Iterative Chip Delay Distribution Calculation

2.6 *Previous Methods*

Figure 3 shows the *iterative* steps of chip delay distribution calculation as discussed in Section 2.2:

It is difficult to calculate statistical MAX distribution (Smax) accurately considering D2D and WID parameter variations. In case of our D2D model, CDF of statistical MAX of two check path delays F1 and F2 (Smax(F1,F2)) is calculated as follows.

$$S\max(F1,F2)(t) = \iiint_{\max(x+f1(z),\, y+f2(z)) \le t} p1(x)\,p2(y)\,p(z) \quad (9)$$

Where $p_1(p_2)$ is WID PDF of $F_1(F_2)$, p is standard Gaussian PDF, $f_1(f_2)$ is D2D model function of $F_1(F_2)$ as (6). It is hard to calculate this integral by numerical methods or Monte Carlo simulations.

In [11], following approximate methods of statistical MAX calculation are proposed.

Previous Method 1: Apply operation (4) to two WID distributions of check path delays. Let this result be WID distribution of statistical MAX. Apply operation (8) to two D2D distributions of path delays. Let this result be D2D distribution of statistical MAX.

Previous Method 2: Apply operation (4) to two total distributions of check path delays. Let this result be statistical MAX distribution.

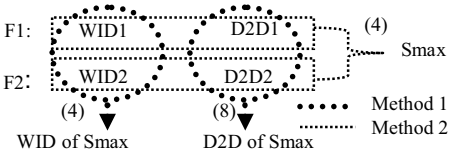

Fig.4. Previous Methods

We can apply these two methods to iterative chip delay distribution calculation. But these methods become inaccurate when the number of check paths becomes larger.

The previous method 1 obtains D2D and WID parameter distributions independently. When the number of check paths becomes larger, this method chooses the smallest negative coefficient (an) of D2D parameter variations from all check paths according to equation (8). However, a check path that has smaller path delay distributions, a small D2D coefficient, tends to have a smaller path delay, which, generally speaking, seldom affects chip delay distributions. Therefore, the negative D2D coefficient of chip delay will be estimated to be pessimistic.

A problem of the previous method 2 is to handle D2D parameter variations, which are correlated, as independent random variables, which causes pessimistic estimation as the number of check paths becomes larger.

III. Proposed Method

In this section we propose a new iterative chip delay distribution calculation method considering D2D and WID variations accurately. In Section 3.1, we propose a new

statistical MAX operation for D2D and WID parameter variations, which will be used in our statistical MAX calculation iteratively.

In Section 3.2, we propose a *path pruning technique* to speed up the statistical MAX operation. A check path which has the delay small enough to be ignored in terms of statistical MAX will be skipped in the operation, because it does not affect chip delay distribution. We introduce the idea of *dominance* to decide which check path should be pruned.

3.1 *Statistical MAX operation*

Fig. 5 shows the basic idea of our proposed statistical MAX operation. For given two paths, the statistical maximum of WID parameter variations and their statistical maximum assuming both D2D and WID parameter variations are calculated. Then, moment matching is used to extract the D2D parameter variations of the two paths from the WID and the statistical maximum. Following are the detailed steps of our proposed statistical MAX operation.

Step1. Apply operation (4) to WID parameter distributions, WID1 and WID2, of the two check paths, F1 and F2. Let this result be WID parameter distribution of statistical MAX.

Step2. Calculate mean (m) and standard deviation (s.d.) of statistical MAX distribution of the check paths, F1 and F2, considering D2D and WID parameter variations, D2D1, D2D2, WID1, and WID2.

Step3. Use moment matching method to calculate D2D coefficients (ap,an) of statistical MAX from means and standard deviations of WID distribution of statistical MAX (Step1) and statistical MAX distribution (Step2).

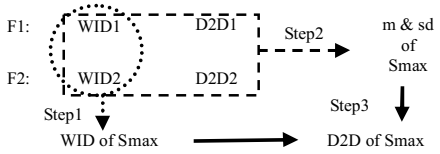

Fig.5. Proposed Smax Operation

Mean (m) and standard deviation (sd) in Step2 are calculated as follows.

$$m = \iiint \max\left(x + f1(z), y + f2(z)\right) p1(x) p2(y) p(z) \qquad (10)$$

$$sd = \iiint \left\{\max\left(x + f1(z), y + f2(z)\right) - m\right\}^2 p1(x) p2(y) p(z) \qquad (11)$$

where symbols in right hand sides are same as integration (9). Monte Carlo simulation or numerical integration, which requires less computational time than integration (9), can be applied to compute the above integrations, (10) and (11).

Details of Step3 are explained in Appendix 1.

Although the proposed method is an approximate calculation, it can obtain more accurate chip delay distributions than previous methods, because not only WID but also D2D parameter variations can be calculated with considering the correlation of D2D parameter variations statistically in Step2.

3.2 *Path Pruning technique with dominance*

In Fig. 3, we define *dominance* of distribution F_i to chip delay distribution D as follows.

$$\textit{Dominance of } F_i = |M_i - M_{i-1}|/M_i \qquad (12)$$

Where, M_i is the mean of distribution of $Smax(F_1,\ldots,F_i)$ and M_{i-1} is the mean of distribution of $Smax(F_1,\ldots,F_{i-1})$. Dominance of F_i shows the magnitude of difference between distribution of $Smax(F_1,\ldots,F_{i-1},F_i)$ and distribution of $Smax(F_1,\ldots,F_{i-1})$ (Fig.6). If dominance of Fi is small enough that we may regard distributions $Smax(F_1,\ldots,F_{i-1},F_i)$ and $Smax(F_1,\ldots,F_{i-1})$ are the same, F_i can be skipped during Step 3 in Fig. 3.

Dominance of F_i can be estimated from statistics of distributions $Smax(F_1,\ldots,F_{i-1})$ and F_n. We set

mc, σc : mean and standard deviation of WID distribution of F_i,

apc, anc : D2D coefficients of F_i,

md, σd : mean and standard deviation of WID distribution of $Smax(F_1,\ldots,F_{i-1})$,

apd, and : D2D coefficients of $Smax(F_1,\ldots,F_{i-1})$,

and assume that WID distribution is Gaussian. Then we get the following estimation.

$$\text{If} \quad k * (\sigma d + \sqrt{\sigma c^2 + h^2}) \le md - mc, \qquad (13)$$

$$\text{then} \quad \text{Dominance} \le A * (3 * \Phi(-k))^{3/4}$$

where h=max(|apc-apd|,|and-anc|), k is any positive constant, Φ is standard Gaussian CDF and A is constant that is derived from the 4th moment and mean of the check path delay distribution (see Appendix2). In practice, 4th moment is obtained from the worst check path delay distribution, and mean from the best check path delay distribution in order to save the computational time of A and to make A pessimistic. We also mention that dominance can be computed analytically from tightness probability [5] if D2D distributions are normal (ap=an).

Our proposed estimation is not mathematically rigorous, because we assume that the check path delay is positive. We believe, however, that this assumption is adequate for the actual circuit data. The details are discussed in Appendix 2.

To prune check paths, a threshold, TH, of dominance is required. Since TH has an impact on the accuracy and CPU time, it should be determined according to the chip designs or applications. TH can be controlled by constant k, and once constant k is fixed, inequality (13) can be used for pruning. We note that the CPU time and the accuracy are trade-off relation. The smaller k is, the larger TH and the number of pruned paths become. Then, the CPU time become smaller and the accuracy become lower.

To be precise, dominance estimation (13) assumes normality of WID distributions. We, however, apply this estimation to non-Gaussian WID as criteria of path pruning heuristics.

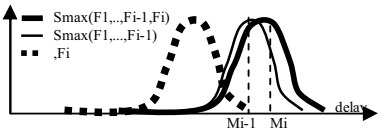

Fig.6. Dominance of delay distribution Fi

IV. Experimental Results

We applied the proposed chip delay calculation to three typical actual chip designs. We selected these chips from a set of chip designs, 130nm to 65nm, based on the path density around critical paths. The number of check paths on each chip is shown in Table 1. The check path sets are selected based on nominal delay criteria.

Table 1. Chip Data [15] ©IEICE 2007

Chip	Number of paths
DataA	60,116
DataB	701
DataC	100,000

We calculate chip delay distributions of these chips with different methods: our proposed method, Monte Carlo simulation method, and previous methods. Monte Carlo results will be used as the reference. The number of intervals for piecewise linear expression for WID distribution is 100. We applied Monte Carlo with 10000 iterations to calculate mean and standard deviation of statistical MAX distribution (See Section 3.1 Step2). The number of iterations for Monte Carlo simulation method was also 10000.

In our experiments, we set k=5 in (13) to obtain the following dominance estimation:

$$5(\sigma d + \sqrt{\sigma c^2 + h^2}) \le md - mc \Rightarrow \text{Dominance} \quad \le 3\times10^{-4}$$

Fig. 7, 8, and 9 show CDF of chip delay obtained by each method.

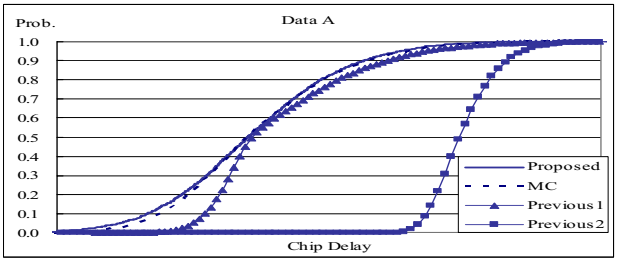

Fig.7 Chip Delay CDF (DataA) [15] ©IEICE 2007

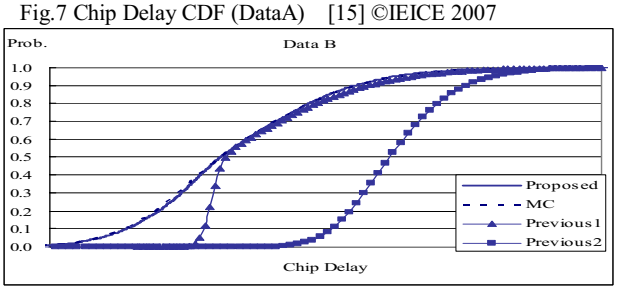

Fig.8 Chip Delay CDF (DataB) [15] ©IEICE 2007

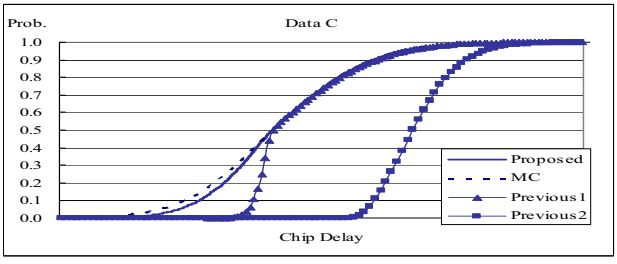

Fig.9 Chip Delay CDF (DataC) [15] ©IEICE 2007

It can be seen from these figures that the CDF from the previous method 2 has large errors because of the reason discussed in Section 2.6. The CDF of the previous method 1 has errors at low probability region (less than 0.5), because the negative coefficient (an) of D2D variation of chip delay tends to be estimated smaller as discussed in Section 2.6. Therefore CDF tends to be sharper at low probability region. On the other hand, the proposed method is accurate even in low probability region, because D2D variations of chip delay are calculated accurately with statistical MAX operation proposed in Section 3.1.

Table 2 shows the CPU time comparison of the proposed method and Monte Carlo.

Table 2.Execution Time (SunOS 1.1GHz) [15] ©IEICE 2007

Chip	Proposed	MC
DataA	51m16s	6h26m42s
DataB	13s	4m29s
DataC	1m06s	10h40m33s

The proposed method is much faster than Monte Carlo because of the pruning technique. Table 3 shows the number of check path selected (i.e., not pruned away) for statistical MAX operation. The number of selected check paths also shows the characteristics of the path density around critical paths.

Table 3. Selected Check Paths [15] ©IEICE 2007

Chip	Number of selected check paths	Rate of selected check paths
DataA	9816	16.3%
DataB	48	6.8%
DataC	184	0.2%

V. Summary and Conclusions

In this paper, we proposed a new iterative method of chip delay distribution calculation considering both D2D and WID parameter variations. The proposed method includes a new statistical MAX operation and a path pruning technique to save the CPU time. We applied the proposed method on three actual chip designs. We showed that the proposed method is more accurate than the previous methods and is faster than Monte Carlo.

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Appendix 1. D2D Coefficient of Statistical MAX

We explain calculation of D2D coefficient of statistical MAX of two check path delay distributions in Step 3 of Section 3.1. We set

- mt,σt: mean and standard deviation of statistical MAX,
- mc,σc: mean and standard deviation of WID distribution of statistical MAX.
- ap, an : D2D coefficients of statistical MAX

Then, mean (m) and standard deviation (sd) of D2D distribution of statistical MAX can be calculated as:

$$m = \frac{(ap - an)}{\sqrt{2\pi}}, \quad sd = \sqrt{\frac{(ap^2 + an^2)}{2} - m^2}$$

The total delay distribution is given by the convolution of D2D delay distribution and WID delay distribution. Then the following equations are derived by moment matching, and give the coefficients ap and an

$$ap - an = A, \quad ap^2 + an^2 = B$$

$$A = \sqrt{2\pi}(mt - mc)$$

$$B = 2(mt - mc)^2 + 2\sigma t^2 - 2\sigma c^2$$

The above equations of 2nd degree of ap and an have the following three cases solution.

Case 1. Two pairs of real solutions

Case 1-1. Such that ap and an of one pair are both positive and those of the other are both negative.

Case 1-2. Such that both ap are positive and both an are negative

Case 2. No real solution.

In case1-1, we choose the coefficient pair which has the same sign as the D2D coefficients of check path delay distribution. In case1-2, we choose the coefficient pair which has larger covariance with D2D distribution of check path delay. The covariance of two D2D distributions whose coefficients are (ap_1,an_1) and (ap_2,an_2) is given by $cov = (ap_1*ap_2+an_1*an_2)/2 + (ap_1-an_1)*(ap_2-an_2)/2\pi$.

In Case2, we choose an and ap by least squares method such that $S(ap,an) = (ap-an-A)^2 + (ap^2+an^2-B)^2$ could be minimum.

Stationary condition of S(ap,an) is as follows.

$$ap + an = 0, \quad 4*ap^3 + 2*(1-B)*ap - A = 0$$

These equations have a real solution such that ap>0 and an<0.

Appendix 2. Estimation of Dominance

We derive the estimation of dominance (16) in Section 3.2. We set that F_i and $Smax(F_1,\ldots,F_{i-1})$ are same distribution as in Section 3.2. D2D and WID parameter distribution functions of those distributions are as follows.

$Smax(F_1,\ldots,F_{i-1})$

p_1:WID PDF, m_1:mean of p_1, σ_1: s.d. of p_1.

ap_1, an_1 : positive and negative D2D coefficients.

F_i

p_2:WID PDF, m_2:mean of p_2, σ_2: s.d. of p_2.

ap_2, an_2 : positive and negative D2D coefficients.

Means of total delay distributions of $Smax(F_1,\ldots,F_{i-1},F_i)$, mt, and $Smax(F_1,\ldots,F_{i-1})$, ms, are calculated as follows.

$$mt = \iiint \max(x + f_1(z), y + f_2(z)) p_1(x) p_2(y) p(z)$$

$$ms = \iiint (x + f_1(z)) p_1(x) p_2(y) p(z)$$

Where p is standard Gaussian PDF.

Let integral domain into $x+f_1(z)>=y+f_2(z)$ and $x+f_1(z)<y+f_2(z)$ divided, then we give

$$mt - ms = \iiint_{x+f1(z)<y+f2(z)} (y + f_2(z)) p_1(x) p_2(y) p(z) - \iiint_{x+f1(z)<y+f2(z)} (x + f_1(z)) p_1(x) p_2(y) p(z)$$

Each integrand of right hand side can be regarded as positive because integrant means delay of a circuit. Therefore, we give following inequality.

$$|mt - ms| \le \iiint_{x+f1(z)<y+f2(z)} (y + f_2(z)) p_1(x) p_2(y) p(z)$$

And by Hoelder inequality ([14], p15), we give following inequality.

$$|mt - ms| \le \left\{ \iiint_{x+f1(z)<y+f2(z)} (y + f_2(z))^4 p_1(x) p_2(y) p(z) \right\}^{\frac{1}{4}} * \left\{ \iiint_{x+f1(z)<y+f2(z)} p_1(x) p_2(y) p(z) \right\}^{\frac{3}{4}}$$

$$\le \left\{ \iiint (y + f_2(z))^4 p_1(x) p_2(y) p(z) \right\}^{\frac{1}{4}} * \left\{ \iiint_{x+f1(z)<y+f2(z)} p_1(x) p_2(y) p(z) \right\}^{\frac{3}{4}}$$

Then, we can estimate dominance as follows.

$$\text{Dominance} \le \left\{ \iiint (y + f_2(z))^4 p_1(x) p_2(y) p(z) \right\}^{\frac{1}{4}} / mt * \left\{ \iiint_{x+f1(z)<y+f2(z)} p_1(x) p_2(y) p(z) \right\}^{\frac{3}{4}}$$

The integral in second bracket on right hand side means the probability that check path delay of F_i is larger than delay of $Smax(F_1,..,F_{i-1})$. Next, we estimate the integral.

$$\iiint_{x+f1(z)<y+f2(z)} p_1(x) p_2(y) p(z) = \iiint_{\substack{z>0 \\ x+a1p*z<y+a2p*z}} p_1(x) p_2(y) p(z) + \iiint_{\substack{z<0 \\ x+a1n*z<y+a2n*z}} p_1(x) p_2(y) p(z)$$

Integrate the right hand side with respect to x with dividing the integral domain into sub-domains that are more or less than the -k-sigma point of p1. Then, we get the following estimate.

$$\le \iint_{\substack{z\ge 0 \\ y+(a2p-a1p)*z>m1-k*\sigma 1}} P_1(y + (ap_2 - ap_1)*z) p_2(y) p(z) + \iint_{\substack{z<0 \\ y+(a2n-a1n)*z>m1-k*\sigma 1}} P_1(y + (an_2 - an_1)*z) p_2(y) p(z) + \Phi(-k)$$

$$\le \iint_{y+(a2p-a1p)*z>m1-k*\sigma 1} p_2(y) p(z) + \iint_{y+(a2n-a1n)*z>m1-k*\sigma 1} p_2(y) p(z) + \Phi(-k)$$

The first term represents the probability that $y + (ap_2-ap_1)*z > m_1 - k*\sigma_1$. The second term represents the probability that $y + (an_2-an_1)*z > m_1-k*\sigma_1$. By assumption, random variable $y+(ap_2-ap_1)*z$ and $y+(an_2-an_1)*z$ are normal and whose means(m) and standard deviations(s.d.) are as followings.

$y+(ap_2-ap_1)*z$: $m=m_2$, $s.d.=sqrt(\sigma_2^2+(ap_2-ap_1)^2)$

$y+(an_2-an_1)*z$: $m=m_2$, $s.d.=sqrt(\sigma_2^2+(an_2-an_1)^2)$

If $m_1 - k*\sigma_1 > m_2+k*sqrt(\sigma_2^2+h^2)$ where $h=max(|ap_1-ap_2|,|an_1-an_2|)$, then the first and second term are less than $\Phi(-k)$ which is the probability that normal random variable is more than the k-sigma point. We give the following estimation.

$$k*(\sigma_1 + \sqrt{\sigma_2^2 + h^2}) < m_1 - m_2$$

$$\Rightarrow \iiint_{x+f_1(z)<y+f_2(z)} p_1(x) p_2(y) p(z) < 3 * \Phi(-k)$$

From this estimation, we give the following dominance estimation in section 3.2.

$$k*(\sigma_1 + \sqrt{\sigma_2^2 + h^2}) < m_1 - m_2$$

$$\Rightarrow \text{Dominance} < A * (3 * \Phi(-k))^{\frac{3}{4}}$$

$$A = \left\{ \iiint (y + f_2(z))^4 p_1(x) p_2(y) p(z) \right\}^{\frac{1}{4}} / mt$$

The numerator of A is the 4th. moment of total delay distribution of Fi [14].