Constraint-free Analog Placement with Topological Symmetry Structure

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Abstract— In analog circuits, blocks need to be placed symmetrically to satisfy the devices matching. Different from the existing constraint-driven approaches, the proposed topological symmetry structure enables us to generate a symmetrical placement without any constraint. Simulated annealing is utilized as the framework of the optimization, and we propose new move operation to maintain the placement's topological symmetry. By inserting dummy blocks, we present a physical skewed symmetry structure allowing non-symmetry partly, so that to enhance the placement on area and wire length. Besides, we incorporate regularity into the evaluation of placement. Experiments shows that our approach generated topological complete symmetry placements without much compromise on chip area and wire length, compared to the placements with no symmetry.

I. INTRODUCTION

In analog circuits, matching the partnered devices helps to avoid both high offset voltage and degradation of power supply rejection ratio [1], so partnered devices are often required to be placed symmetrically.*Constraint-driven* approaches[3],[5], [7], [8] can yield placements satisfying the matching requirement . Since no efficient generation of constraint has been established yet, constraint is generated manually, the *constraint-driven* approaches still suffer from the time-consuming constraint generation process.

The structured placement proposed in [11] is a constraint-less approach to pursue the regularity of analog placement. Following this constraint-less concept, we introduce another structured placement focusing on topological symmetry structure. Our contribution is summarized as follows.

- Not specifying any block's name, we can formulate the topological complete symmetry structure. Based on this structure, the placement goes to symmetry naturally without any constraint. Besides, this structure enables us to calculate the vertical coordinate in the linear time to the number of edges of the constraint graph.

- We introduce the physical skewed symmetry structure for sacrificing the complete symmetry against minimizing the area or wire length.

In order to improve the placement, we utilize simulated annealing as a framework of the optimization process and propose efficient moves to maintain the topological symmetry at every step. Furthermore, we introduce zero-size dummy blocks to

present *Physical Skewed Symmetry Structure*. As a result, we can release physically symmetry to get the placement with less area or wire length.

In experiments, we applied our structured placement to industrial instances for analog block designs. In addition, we combine the evaluation of symmetry structure with the evaluation procedure introduced in [11] for taking row and array structures into consideration. In the results, the placements of the complete symmetry structure could be obtained by the compromise of about 5% on average with respect to the chip area and the wire length, compared to the placements with no symmetry. Furthermore, we tested the ability of physical skewed symmetry placement. Those inserted dummy blocks endue other blocks more flexibility, and serve to reduce the chip area and wire length as expected.

The rest of this paper is organized as follows. Section II describes preliminary concepts of our structured placement. Section III introduces the topological property of a topological complete symmetry. Section IV describes the framework of the optimization of placement with new move, and introduces the physical skewed symmetry structure. Section V demonstrates the experimental results. Section VI concludes contribution and future work.

II. SEQUENCE-PAIR & SINGLE-SEQUENCE

A sequence-pair [2] is an ordered pair of Γ_+ and Γ_- to represent a placement. Each of Γ_+ and Γ_- is a permutation of names of given n blocks. If block x is the i-th in Γ_+, we denote $\Gamma_+(i) = x$, as well as $\Gamma_+^{-1}(x) = i$. Similar notation is also used for Γ_-. For every block pair (a, b), a is the left of b (equivalently, b is the right of a) if $\Gamma_+^{-1}(a) < \Gamma_+^{-1}(b)$ and $\Gamma_-^{-1}(a) < \Gamma_-^{-1}(b)$. Analogously, a is below b (equivalently, b is above a) if $\Gamma_+^{-1}(a) > \Gamma_+^{-1}(b)$ and $\Gamma_-^{-1}(a) < \Gamma_-^{-1}(b)$.

The single-sequence [4], [6], [9], [10] can represent a placement's topology without specifying block's name. It is defined as $\mathcal{S}(k) = \Gamma_+^{-1}(\Gamma_-(k))$, that is, $\mathcal{S}$ is the same as Γ_- when each block is renamed as $\Gamma_+ = (1, 2, \ldots, n)$.

III. TOPOLOGICAL SYMMETRY STRUCTURE

Symmetry structures are required in analog placement to match device pairs. Related works in [3], [7] introduce constraint-driven approaches to realize a placement satisfying the symmetry requirement.However, the specification of the

Fig. 2. An example of generation of symmetry structure.
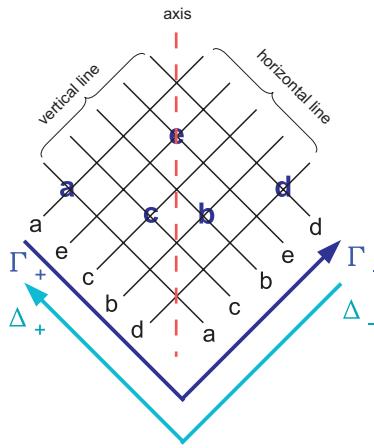
Fig. 1. An example of sequence-pair with horizontal symmetry topology.

constraint is a tough task, and no efficient generation of appropriate constraint has been established yet. Therefore, we introduce the generation of symmetry structures without specifying any pair of devices or name of any block. It is possible that a placement naturally goes to a symmetry structure.

Let a sequence-pair be $\mathcal{SP} = (\Gamma_+, \Gamma_-)$, and let the reverse sequences of Γ_+ and Γ_- be Δ_+ and Δ_-, respectively. Originally, a sequence-pair is defined by the arrangement of blocks from the left-side to the right-side over the chip. We call such a sequence-pair *LR-SP*. On the other hand, if a sequence-pair is defined from the right-side to the left-side, the sequence-pair is called *RL-SP*. We notice that *RL-SP* is (Δ_-, Δ_+). $\Gamma_+(k)$ and $\Delta_+(n-k+1)$ correspond to the same block as well as $\Gamma_-(k)$ and $\Delta_-(n-k+1)$ do to the same one.

If the *LR-SP* and *RL-SP* induce the same single-sequence, that is,

$$\Gamma_+^{-1}(\Gamma_-(k)) = \Delta_-^{-1}(\Delta_+(k)), \qquad (1)$$

then we say that the sequence-pair has a *horizontal symmetry topology*.

Given an $n \times n$ grid, assigning n blocks into the grid according to (Γ_+, Γ_-) will result in the corresponding placement. Denote k as j, denote $\Gamma_+^{-1}(\Gamma_-(k))$ and $\Delta_-^{-1}(\Delta_+(k))$ as i. The equation (1) means that if a block was assigned to the joint of i-th horizontal line and the j-th vertical line, another block(or itself, if it is on the axis) will appear on the symmetric position which is the joint of reversed i-th vertical line and the reversed j-th horizontal line. The symmetry axis is the diagonal of the grid. Fig. 1 shows an example, the grid has been rotated 45 degree. The *LR-SP*$(\Gamma_+, \Gamma_-) = (aecbd, acbed)$ and the *RL-SP*$(\Delta_-, \Delta_+) = (debca, dbcea)$ introduce the same single-sequence which is (13425), so the sequence-pair has a *horizontal symmetry topology*

In the following, we introduce the generation of a single-sequence with an arbitrary horizontal symmetry topology. A horizontal symmetry topology has a single vertical axis. It can be also extended to a horizontal axis or plural axes, but the extension is omitted here for the space limitation. An example
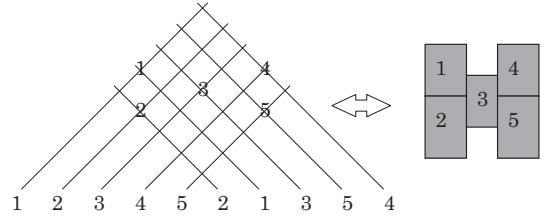
is shown in Table I and Fig. 2. $\Gamma_-(k)$ and $\Delta_+(k)$ (or $\Gamma_+(k)$ and $\Delta_-(k)$) correspond to a symmetry-pair. Note that if they correspond to the same block, it means a self-symmetry.

1. Make a check-list of $(1, 2, \ldots, n)$. Set Γ_+ as $(1, 2, \ldots, n)$, Δ_+ as $(n, n-1, \ldots, 1)$, Γ_- and Δ_- as empty, and $k = 1$.

2. Stop the procedure if all numbers have been assigned to Γ_-, that is, the check-list is empty.

3. Assign an arbitrary number x in the check-list to $\Gamma_-(k)$, and remove x from the check-list.

4. Assign $n - k + 1$ to both $\Delta_-(x)$ and $\Gamma_-(n - x + 1)$, and remove $n - k + 1$ from the check-list.

5. Increment k until $\Gamma_-(k)$ has not been assigned to, and return to step 2).

Furthermore, in the table, $x = 2$ and $x = 1$ are chosen arbitrarily (see step 3) above). If we take other choices, the resultant Γ_- would be different. In other words, we can control the generation of a single-sequence with a horizontal symmetry topology by choosing these numbers.

TABLE I
AN EXAMPLE OF SINGLE-SEQUENCE GENERATION WITH A HORIZONTAL SYMMETRY TOPOLOGY.

k	x	$n-k+1$	$n-x+1$	Γ_- and Δ_-	check-list
		initial		(-, -, -, -, -)	(1, 2, 3, 4, 5)
1	2	-		-	(2, -, -, -, -)	(1, 3, 4, 5)
1	2	5	4	(2, -, -, 5, -)	(1, 3, 4)
2	1	-		-	(2, 1, -, 5, -)	(3, 4)
2	1	4	5	(2, 1, -, 5, 4)	(3)
3	3	-		-	(2, 1, 3, 5, 4)	(-)

Consider the realization of a symmetry placement from a sequence-pair with a horizontal symmetry topology. Prior works [3], [7] introduce a special calculation to place a pair of blocks imposed a symmetry-constraint on so that the y-axis becomes the center between them and their y-coordinates are the same [3], [7]. But, they suffer from the time-consuming calculation of y-coordinates, because it often needs several iterations to align y-coordinates of a horizontal symmetry-pair. However, we can give a single path calculation of y-coordinates of symmetry-pairs as long as the sequence-pair has a horizontal symmetry topology.

Theorem III.1 *(Vertical Feasibility) For each symmetry-pair, if their y-coordinate is the same coordinate in the placement,*

the placement is called vertical feasible. *A vertical constraint graph induced by a sequence-pair with a horizontal symmetry topology is given. It has no directed cycle. Y-coordinate of every block of a vertical feasible placement can be calculated in the time complexity that is linear to the number of edges of the constraint graph.*

IV. SYMMETRY-ORIENTED OPTIMIZATION

Simulated annealing is adopted as the optimization framework. In the following, we will describe (i) generation of an initial placement, (ii)evaluation of symmetry, (iii) cost function, (iv) move operation, (v) physical skewed symmetry structure.

A. Generation of Initial Placement

As we described above, we can generate a single-sequence satisfying a topological complete symmetry. Let the single-sequence be $\mathcal{S}_{symm}$. We assign blocks to $\mathcal{S}_{symm}$, then generate the initial placement. Note that this assignment corresponds to the configuration of a sequence-pair. If two number consist one symmetry-pair, one number calls the other *partner*. In this assignment, blocks are classified according to their size so that blocks of the similar size belong to the same group. Hence, every block is assigned to $\mathcal{S}_{symm}$ such that the partner is chosen from the same group.

$\mathcal{S}_{symm}$ consists of a set of symmetry-pair numbers and self-symmetry numbers. We set a limitation on the amount of self-symmetry numbers in order to avoid too much self-symmetry blocks. Although our concept is constraint-less, we are still able to combine the constraint-driven approach to our placement. For a particular pair of blocks should be symmetrical, i.e. they need to satisfy one symmetry constraint, we assign them into a symmetry-pair numbers, make them as the partner of each other.

B. Evaluation of Symmetry

Topological structure value V_{top} and *Physical dimension cost* C_{phy} introduced in [11] are used to evaluate the quality of a structured placement. Multi-rows and arrays are extracted so the two values involving some factors such as local compactness can be calculated. Since we can control the generation of the initial symmetry placement, the symmetry structures can be extracted during the generation, then those factors of symmetry structures can be also calculated.

Given a symmetry x, $|x|$ denotes the number of blocks and $|x_{self}|$ denotes the number of self-symmetry blocks. The width and the height of a block b are denoted by $w(b)$, $h(b)$ respectively. The topology of a symmetry x is valued as:

$$V_{top}(x) = |x| - |x_{self}|; \qquad (2)$$

and the local symmetricity of a symmetry x is valued as:

$$C_{sym}(x) = \sum_{(b,b' \in x)} |w(b) - w(b')| * |h(b) - h(b')|. \qquad (3)$$

Although in this paper we focus on the symmetry of a placement, multi-rows and arrays are still preferred in an analog layout, so we combine the factors of symmetries into V_{top} and

C_{phy}. Let sets of arrays, multi-rows and symmetries be A, R and X, respectively.

- The *Topological structure value* is defined as:

$$V_{top} = \alpha * \sum_{r \in R} \sigma(r) + \beta * \sum_{a \in A} \sigma(a) + \gamma * \sum_{x \in X} (|x| - |x_{self}|), \qquad (4)$$

where the first two items in formula(4) are the same in [11], σ figures out the aspects of arrays and multi-rows. α, β and γ are coefficients to balance a trade-off among structure values.

- The *Physical dimension cost* is defined as:

$$C_{phy} = \begin{array}{l} \alpha' * \sum_{a \in A} (C_{cmp}(a) + C_{uni}(a)) \\ + \beta' * \sum_{r \in R} (C_{cmp}(r) + C_{uni}(r)) \\ + \gamma' * \sum_{x \in X} C_{sym}(x), \end{array} \qquad (5)$$

where the first two items in formula(5) are the same in [11], C_{cmp} and C_{uni} describe the local compactness and uniformity respectively, α', β' and γ' are coefficients to balance a trade-off among costs.

V_{top} contributes to describe the topological shape of a placement and C_{phy} does to describe the local compactness and uniformity.

C. Cost Function

Our cost function E for a placement P is designed as follows.

$$E(P) = \frac{Area(P) \cdot WLen(P)}{g(V_{top})} * g(C_{phy}),$$

where $Area(P)$ and $WLen(P)$ are the chip area and the wire length of P, respectively. g is a conversion that maps an input value to another value within $[1.0, 1.1)$, and it is defined as: $g(x) = 1.0 + 0.1 \exp(\frac{x_m \ln(0.5)}{x + \epsilon})$, where x_m is an average value of $\{x\}$ and ϵ is a small value enough to ignore. The meaning of the function g is to be likely to degrade the chip area or the wire length by 10% to obtain better topological structure value or less physical dimension cost.

D. Moves Keeping Symmetry

We propose new moves to maintain the topological symmetry during an annealing process. For every move, we choose two blocks a and b. Our moves are explained as a combination of FullExchange(a, b) and HalfExchange(a, b) introduced in [2]. For the completeness, we briefly described these moves.

- FullExchange(a, b): Pair interchange of names of two block a and b in both Γ_+ and Γ_-.

- HalfExchange(a, b): Pair interchange of two blocks names in either Γ_+ or Γ_-.

In the following, we describe all the moves used in a simulated annealing. The simulated annealing controls the selection of moves according to random values.

A: FullExchangeOfSymm on block a and b

B: HalfExchangeOfSymm on block a and b
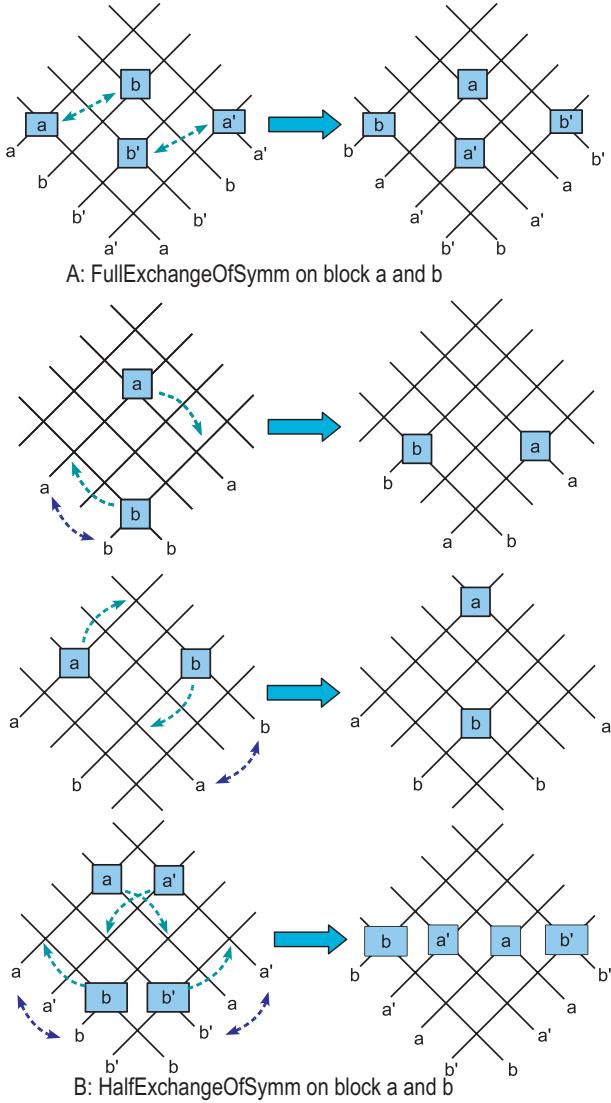
Fig. 3. Moves Keeping Symmetry.

1. RotateBlock(a): Rotate the block a by 90 degree.

2. FlipBlock(a): Flip the block a horizontally.

3. FullExchangeOfSymm(a, b): Let partners of a and b be a' and b', respectively. If a' is equal to b, apply FullExchange(a, b) introduced in [2]. Otherwise, apply both FullExchange(a, b) and FullExchange(a', b'). An example is shown in Fig. 3(A).

4. HalfExchangeOfSymm(a, b): Let partners of a and b be a' and b', respectively. If a and b are a symmetry-pair or two self-symmetry blocks, apply HalfExchange(a, b) introduced in [2]. Note that in this exchange, two self-symmetry blocks will be turned into a symmetry-pair, while a symmetry-pair will be separated into two self-symmetry blocks. Otherwise, apply HalfExchange(a, b) on Γ_+(or Γ_-) and HalfExchange(a', b') on Γ_-(or Γ_+). An example is shown in Fig. 3(B).

A: complete topological symmetry

B: non-complete topological symmetry


C: Put dummy blocks to get skewed symmetry
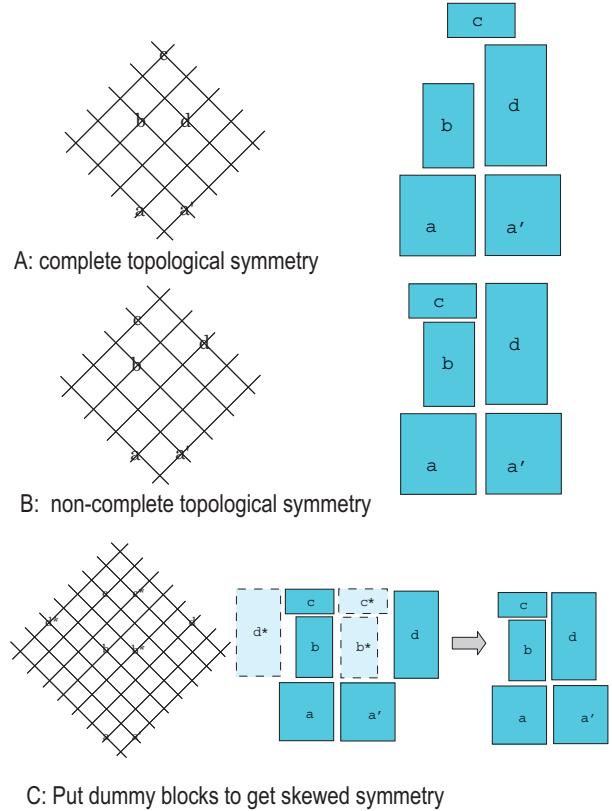
Fig. 4. Physical Skewed Symmetry Structure.

E. Physical Skewed Symmetry Structure

Because of the limitation of the block's size or shape, a complete symmetry placement may lead to too much compromise on chip area and wire length. Fig. 4 shows an example with 5 blocks: a, a', b, c, and d. a and a' have the same size and shape. A complete symmetry-oriented placer trends to get a placement like Fig. 4(A) which is complete topological symmetry, but might not so good at the area. But there could be another solution like Fig. 4(B), which can not be obtained by a complete symmetry placement, but the placement still looks symmetry because the area of it's left side and right side are almost same. In order to make improvement on those topological complete symmetry placement, we insert some dummy blocks into the single-sequence, and the size of each dummy block is 0. In a symmetry structure, if a block's symmetry partner is a dummy block, we say that they formulate a *Physical Skewed Symmetry Structure*.

During the generation of the initial placement and the optimization, the single-sequence keeps being topological symmetry. The dummy blocks are ignored in the symmetry coordinate calculation, so it is possible to generate a physical skewed symmetry placement including non-symmetry parts. As a result we may get a more compact placement. In Fig. 4(C), dummy blocks b^*, c^* and d^* are inserted into the single-sequence, and form a topological complete symmetry placement, finally help to lead to the result like Fig. 4(B).
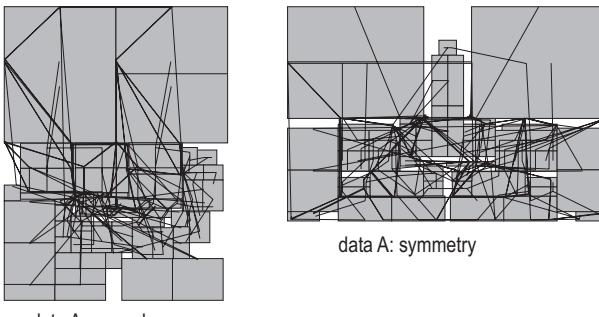
data A: normal
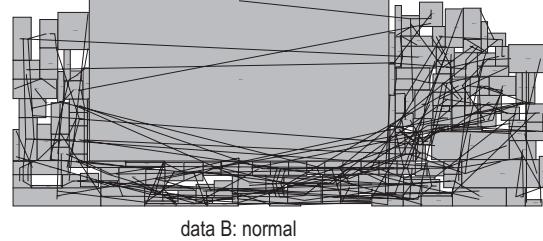
data A: symmetry

data B: normal

data B: symmetry

Fig. 5. Resultant placements of data A, B, where the primary objective is the product of the chip area and the wire length: "normal" and "symmetry" are normal placement and our symmetry placement respectively.
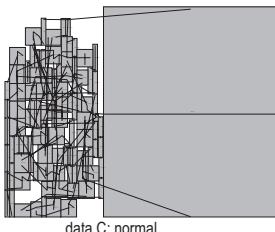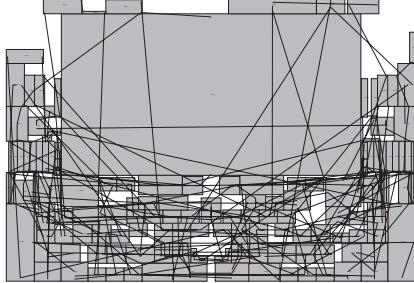
data C: normal
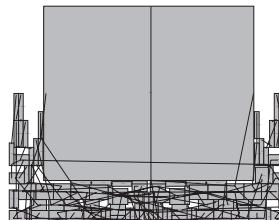
data D: normal

data C: complete symmetry

data D: complete symmetry
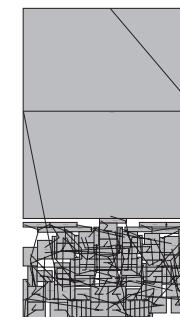
data C: physical skewed symmetry
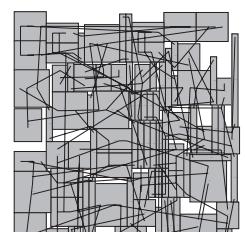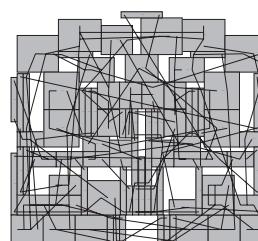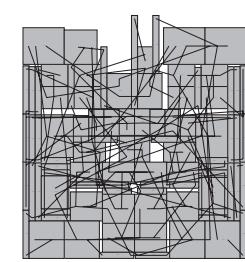
data D: physical skewed symmetry

Fig. 6. Resultant placements of data C and D, where "normal", "complete symmetry" and "physical skewed symmetry" are normal placement, complete symmetry placement and physical skewed symmetry placement respectively.

V. Experiments

We implemented our symmetry-oriented structured placement, and performed it on 14 instances of analog block sets from industries. A normal block placement based on sequence-pair was also implemented.

A. Comparison with normal placement

First, we compare our structured placement with normal one. Fig. 5 shows two pairs of resultant placements. The results of normal placement are well compacted, but not well organized in local area, and lack symmetry. Our symmetry structured placement is well compacted either and distinguishes for the perfect symmetry generated without any constraint. Since we combined the evaluation of row and array structures, our placement also shows good quality on local compactness and regularity. Our placement is strictly limited to be symmetrical, but the chip area and the wire length are not necessarily increasing heavily due to this limitation. The numerical results are shown in Table II. The normal placement and our placement are denoted by *normal* and *symm* respectively. The table includes the results about the chip area and the wire length by both placements. The results show, as we expected, our placement with a complete symmetry structure could be obtained by the compro-

mise of at most about 5 % on average, compared to the normal placement.

B. Physical Skewed Symmetry

Secondly, we demonstrate the effectiveness of *physical skewed symmetry* structure. For the same instances, we generated the dummy blocks as the 10%, 20%, and 30% of the number of input blocks, and tested each case. The numerical test result is shown in Table III. In this table, values about chip area and wire length are ratios to the chip area and wire length by *symm* in Table II. The columns of "Best" show the best result among the those of "dummy 0%", "dummy 10%", "dummy 20%" and "dummy 30%". We attained the 6% and 14% reduction on average with respect to chip area and wire length. Fig. 6 shows the result by *normal*, *complete symmetry* and *physical skewed symmetry*. We are convinced that the insertion of the dummy blocks expands the solution space of the symmetry-oriented placement, and helps to reduce the chip area and wire length.

VI. Conclusion

This paper presented a structured placement focusing on topological symmetry structure. Unlike the existing constraint-driven approach, it does not need any constraint. We formu-

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TABLE II

THE NUMERICAL RESULT OF ANALOG BLOCK DESIGNS, WHERE "WLEN" IS THE WIRE LENGTH, "NORMAL" AND "SYMMETRY" REFER TO NORMAL PLACEMENT AND OUR SYMMETRY PLACEMENT RESPECTIVELY.

data	#blocks	#nets	normal			symm			(symm-normal)/symm	
			area(μm^2)	wlen(μm)	time(sec)	area(μm^2)	wlen(μm)	time(sec)	area(%)	wlen(%)
A	122	91	102,660	9,356	1,581	107,940	10,444	840	5.14	11.63
B	60	46	80,784	5,391	241	100,082	7,007	221	23.89	29.98
C	113	80	265,068	16,520	1,261	257,420	14,820	684	-2.89	-10.29
D	32	22	69,090	2,413	49	74,844	3,120	75	8.33	29.30
E	54	49	67,077	3,286	172	71,760	3,023	177	6.98	-8.01
F	90	58	94,105	9,680	700	103,968	9,786	497	10.48	1.10
G	64	49	58,622	5,274	263	60,543	6,043	258	3.28	14.58
H	66	29	173,631	4,124	632	193,953	3,699	534	11.70	-10.30
I	60	36	12,683	2,465	236	13,008	2,530	238	2.56	2.61
J	166	105	75,507	15,576	7,926	80,565	12,645	1,600	6.70	-18.82
K	55	91	865,860	38,209	376	916,491	36,717	449	5.85	-3.91
L	101	78	42,452	3,392	1,868	45,456	4,692	1,148	7.08	38.31
M	22	53	543,753	8,390	29	497,151	10,107	56	-8.57	20.46
N	60	44	159,799	3,715	463	163,681	3,010	352	2.43	-18.97
average:									5.93	5.55

TABLE III

THE NUMERICAL RESULT OF ANALOG BLOCK DESIGNS USING *Physical Skewed Symmetry Structure*.

data	dummy 0%		dummy 10%			dummy 20%			dummy 30%			Best(0–30%)	
	area	wlen	#dummy	area(%)	wlen(%)	#dummy	area(%)	wlen(%)	#dummy	area(%)	wlen(%)	area(%)	wlen(%)
A	100	100	12	91.2	111.7	24	102.3	106.6	36	98.6	113.3	91.2	100
B	100	100	6	91.1	75.7	12	91.2	83.2	18	85.5	81.7	85.0	75.7
C	100	100	11	124.9	104.7	22	125.5	98.4	33	114.2	99.8	100	98.4
D	100	100	3	96.9	130.4	6	98.3	103.9	9	96.4	83.3	96.4	83.3
E	100	100	5	109.0	97.3	10	99.2	108.5	16	98.6	108.7	98.6	97.3
F	100	100	9	89.3	103.3	18	95.9	96.6	27	94.4	96.4	89.3	96.4
G	100	100	6	99.8	98.5	12	100.8	95.4	19	102.5	106.7	99.8	95.4
H	100	100	6	112.5	84.4	13	100.8	85.4	19	99.4	91.8	99.4	84.4
I	100	100	6	84.2	80.6	12	90.3	82.6	18	96.5	76.0	84.2	76.0
J	100	100	16	102.2	107.3	33	98.6	73.2	49	99.6	94.7	98.6	73.2
K	100	100	5	98.2	93.2	11	129.5	153.9	16	96.2	105.3	96.2	93.2
L	100	100	10	89.8	81.4	20	90.6	85.3	30	89.2	75.9	89.2	75.9
M	100	100	2	106.1	113.9	4	104.6	63.9	6	100.2	73.2	100.0	63.9
N	100	100	6	94.0	141.3	12	98.7	118.5	18	101.7	109.4	94.0	100.0
average				99.2	101.7		101.9	96.8		98.0	94.0	94.4	86.6

lated the property of a topological complete symmetry in terms of single-sequence. Besides, we proposed an efficient move used in a simulated annealing to maintain the topological symmetry of every placement. Furthermore, we introduced physical skewed symmetry structure to compromise symmetry for less chip area or wire length. In experiments, we showed that our approach generated topological complete placements without much compromise on chip area and wire length, compared to the placements with no symmetry.

In future works, we are going on studying the structured placement with hierarchical regular structures such as array, row, and symmetry.

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