Parameterized Embedded In-circuit Emulator and Its Retargetable Debugging Software for Microprocessor/Microcontroller/DSP Processor

Liang-Bi Chen, Yung-Chih Liu, Chien-Hung Chen, Chung-Fu Kao, and Ing-Jer Huang

Department of Computer Science and Engineering
National Sun Yat-Sen University
Kaohsiung, 80424, Taiwan, R.O.C.
Tel : 886-7-5254337
Fax : 886-7-5254301
e-mail : {liangbi, ijhuang}@cse.nsysu.edu.tw

Abstract - The in-circuit emulator (ICE) is commonly adopted as a microprocessor debugging technique. In this paper, a parameterized embedded in-circuit emulator and its retargetable debugging software are proposed. The parameterized embedded in-circuit emulator can be integrated into different style processors such as microcontroller, microprocessor, and DSP processor. The GUI interface debugging software can help user to debug easily. As a result of it, the duration of microprocessor debugging design procedure time is reduced.

I. Introduction

An in-circuit emulator (ICE) is part of the development environment for microprocessor (or microcontroller1)-based systems (called *target systems*). An ICE, while retaining the same functionality as the original microprocessor, provides extra debugging and testing mechanisms such as single stepping, break point setting and detection, internal resource monitoring and modification, *etc*., to support designers in the development/maintenance of the hardware and software of the target systems. An embedded in-circuit emulator (EICE) is an ICE embedded in the processor's core so that the ICE functions can be applied to the core. By incorporating the JTAG facilities, the EICE needs not additional pins. It is called EICE due to its permanent incorporation within the SoC chip. The EICE has been implemented in the many chips such as ARM7TDMI [1]. However, the architecture of EICE is fixed for fixed processor architecture and the fixed set of instructions. The drawback of the fixed EICE is that it consumes die size and is not reusable. Hence, we propose a parameterized embedded in-circuit emulator and its retargetable debugging software in order to reduce the debugging design procedure time for different target systems. The parameterized embedded in-circuit emulator can be integrated to different style processors such as microcontroller, microprocessor, and DSP processor. The GUI interface debugging software can help user to debug easily.

II. Retargetable Embedded ICE Hardware/Software Module Design

A. Parameterized Embedded ICE Design

Our parameterized EICE is based on IEEE 1149.1 JTAG standard. Fig.1 shows the architecture of the EICE. When the clock of microprocessor core is halted, TCK, TMS of TAP controller signals can be used to input breakpoint data in Breakpoint Scan Register (BSR) from TDI pin. Then BSR will set one of several set breakpoints in Breakpoint Detect Unit (BDU). When we set the EICE in Monitor (Debug) mode, the clock will be allowed to supply microprocessor core and BDU will detect whether the processor matches the breakpoint condition. If match, breakpoint detection unit will enable a breakpoint signal to disable the normal execution of the microprocessor at a specific time. Then the microprocessor will be in the TAP mode, and the debug and test circuit will execute the command coming from the debug host (i.e. PC or workstation). The EICE needs two signals *eoi* (end-of instruction) and *flush* from microprocessor core for timing control of stopping system clock. The *eoi* (end of instruction) is active when the instruction finishes. The *flush* is active when branch happens; this indicates that microprocessor would flush instruction fetched in pipeline. This signal is supported by core designer.

B. Retargetable Debugging Software Design

Fig. 2 shows retargetable EICE debugging software. The processor information setup file and the ICE information setup file should be provided by the processor designer according to the processor designer's requirements.

III. Experiment Results

We have been successfully demonstrated by integrating EICE with several processors with significantly different architectures: one 8-bit industrial microcontroller HT48x00, one 32-bit ARM7-like embedded microprocessor, and one 32-bit ITRI PAC DSP processor. FPGA prototypes and chip implementation have been accomplished.

Fig. 3 shows the FPGA prototyping of retargetable EICE hardware/software. We can also design a prototype which can be connected via ARM multi-ICE to verify correctness and

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compatibility of our EICE design, which is shown in Fig.4. In this case study, the UMC 0.18μm technology and the Artisan cell library are used to synthesize the 32-bit ARM7-like microprocessor with EICE integrated on the ARM EASY (Example AMBA SYstem) environment [3] as shown in Fig.5. Table 1 summarizes the synthesis result and Fig. 6 shows the chip layout.

IV. Conclusion

In this paper, we propose a parameterized embedded in-circuit emulator and its retargetable debugging software in order to reduce the debugging design procedure time for the different target systems. The goal is to integrate the EICE component into the microcontroller/microprocessor/DSP processor, and to execute debugging functions via proposed retargetable GUI debugger tool. As a result of it, the duration of debugging procedure and time-to-market is reduced.

References

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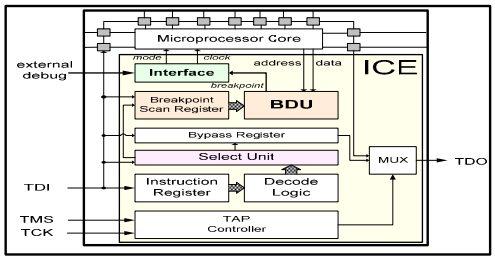

Fig. 1. EICE Architecture

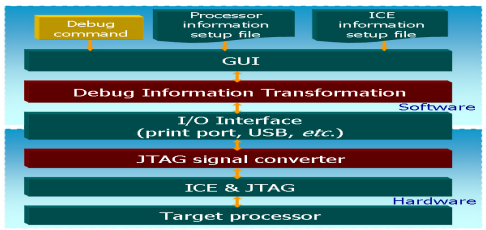

Fig. 2. Retargetable EICE debugging software

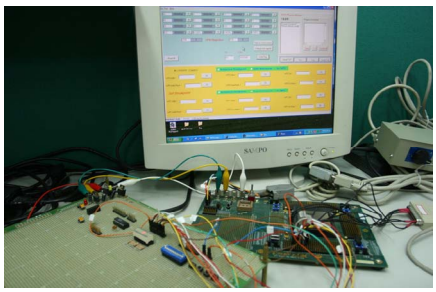

Fig. 3. FPGA prototyping of retargetable EICE hardware/software

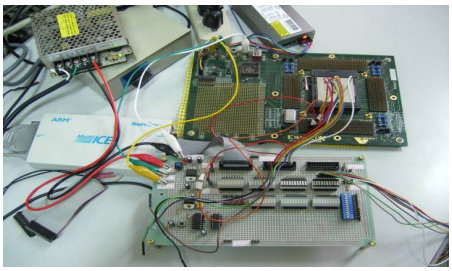

Fig. 4. FPGA prototyping for ARM debugging tool chain

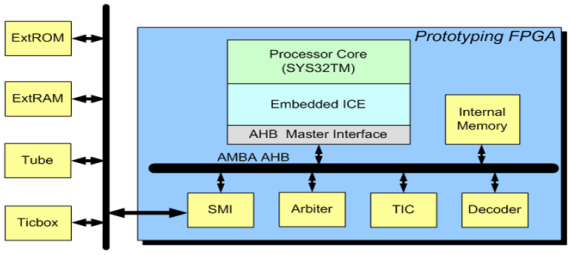

Fig.5. ARM7-like μP with EICE is integrated on the ARM EASY

TABLE I

Synthesis result of a 32-bit ARM7-like processor with an EICE is integrated on the AMBA-AHB Bus

Technology	**UMC 0.18μm 1P6M**
Core Size	2.9x2.9 mm^2
On-chip memory	8KB SRAM
Power consumption	30mW @ 66MHz
Number of pins / package	160 / CQFP160

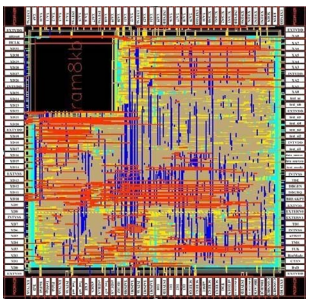

Fig. 6. Chip layout