Small-Area CMOS RF Distributed Mixer Using Multi-Port Inductors

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***Abstract*— This paper presents a novel small-area distributed mixer for ultrawide-band (UWB) receivers. The proposed mixer uses five 4-port inductors instead of fifteen 2-port inductors to shrink area of the circuit. The proposed mixer achieves conversion gain of -10 dB, noise figure of 15 dB, return loss of less than -10 dB from 2.3 to 6.0 GHz, IIP3 of 13.6 dBm, and the circuit area of 0.51 mm^2.**

I. Introduction

Ultrawide-band(UWB) wireless interconnection are capable of carrying huge amounts of data of more than 480 Mbps for personal area network (PAN) [1]. Because of the spread spectrum characteristics of UWB, amplifiers and mixers covering wide band are necessary. Distributed mixers has been proposed as wide-band mixers [2], [4], [5]. The area are, however, very large. This paper presents a small-area distributed mixer using multi-port inductors.

II. Small-Area Distributed Mixer

Figure 1 shows a schematic of distributed mixer. The conventional distributed mixer consists of input- and output-port transmission lines and metal oxide semiconductor field effect transistors (MOSFETs). Transmission lines are usually implemented by LC ladders to reduce circuit area.

In the conventional distributed mixer shown in Fig. 1, input- and output-port LC ladders are constructed by 2-port spiral inductors and capacitors. The capacitors in input-port ladder are substituted by gate capacitances C_{gs} of MOSFETs.

Cut-off frequency (f_c) and characteristic impedance(Z_0) of the LC ladder are calculated by the following equations [3].

$$f_c = 1/(\pi\sqrt{LC}) \quad (1)$$

$$Z_0 = \sqrt{L/C} \quad (2)$$

The inductance L and capacitance C of the LC ladder are determined by Eq. (1) so that f_c is equal to the maximum frequency of distributed mixer. Characteristic impedance Z_0 is designed to be 50 Ω by Eq. (2)

In conventional distributed mixers, several 2-port inductors are necessary for LC ladder, and they occupies large chip area. The circuit area can be decreased by using multi-port inductors reported in [11]. Three 2-port inductors can be replaced with a 4-port inductor shown in Fig. 2. In case of 2-stage distributed mixer, fifteen 2-port inductors are replaced with five 4-port inductors as shown in Fig. 2. Thus, the circuit area can be reduced.

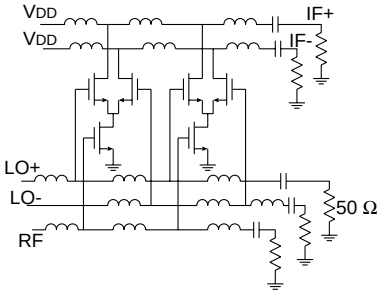

Fig. 1. Schematic of 2-stage distributed mixer.

Figure 3 shows equivalent circuit of the 4-port inductor. L_{12} is defined as inductance between ports 1 and 2, L_{23} and L_{34} are alose defined by the same rules. R_{12}, R_{23} and R_{34} are DC resistances of the inductor. Each C_{oxn} represents capacitance between wire line and ground. C_{Sin} and R_{Sin} are substrate capacitance and resistance. These parasistic components can be neglected in frequency range up to about 6 GHz. Mutual coupling of each segment is considered. Inductance and quality factor of wiring between port l and m are calculated as follows.

$$L_{lm} = 1/(2\pi f)\cdot \mathrm{Im}\left(z_{ll} - z_{lm}z_{ml}/z_{mm}\right) \quad (3)$$

$$Q_{L_{lm}} = \left\{\mathrm{Im}\left(z_{ll} - z_{lm}z_{ml}/z_{mm}\right)\right\} / \left\{\mathrm{Re}\left(z_{ll} - z_{lm}z_{ml}/z_{mm}\right)\right\} \quad (4)$$

where z_{ij} represents elements of z-parameter, f is frequency. Each k is calculated as follows.

$$M_{L_{lm}L_{mn}} = \left\{L_{ln} - (L_{lm} + L_{mn})\right\}/2 \quad (5)$$

$$k_{L_{lm}L_{mn}} = M_{L_{lm}L_{mn}} / \sqrt{L_{lm}L_{mn}} \quad (6)$$

where L_{ln} is self inductance between ports l and n. $M_{L_{lm}L_{mn}}$ is mutual inductance between L_{lm} and L_{mn}. $k_{L_{lm}L_{mn}}$ is coupling coefficient between L_{lm} and L_{mn}.

Figure 4 (a) shows simulated self inductances. L_{12} is 0.5 nH, L_{23} is 1.0 nH at 6 GHz. L_{34} have similar value as L_{12} according to its symmetry structure. Figure 4 (b) shows simulated quality factor. Each quality factor is about 8.0 at maximum. Figure 4 (c) shows simulated coupling coefficient. $k_{L_{12}L_{23}}$ is about 0.4, $k_{L_{13}L_{34}}$ is about 0.6. $k_{L_{23}L_{34}}$ have similar value as $k_{L_{12}L_{23}}$ according to its symmetry structure.

III. Measurement Result

A two-stage distributed mixer was designed and fabricated by 6-layer 0.18 μm CMOS process. Figure 5 shows the micrograph of the mixer. The size of the distributed mixer is 0.85 mm × 0.6 mm(= 0.51 mm^2).

The performance characteristics of mixer can be divided into four parameters: conversion gain, return loss, noise figure and IIP3 [12].

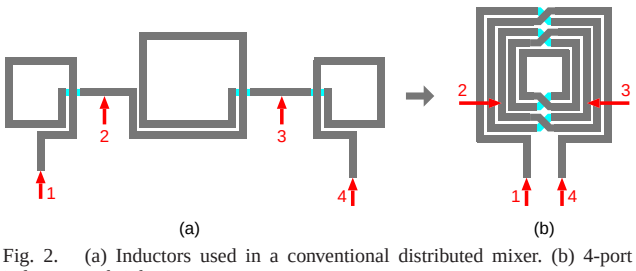

Fig. 2. (a) Inductors used in a conventional distributed mixer. (b) 4-port inductor to shrink circuit area.

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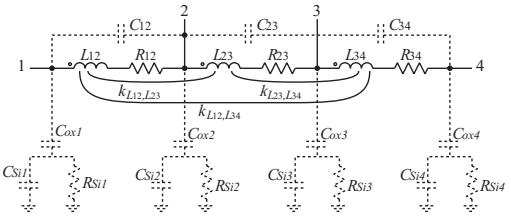


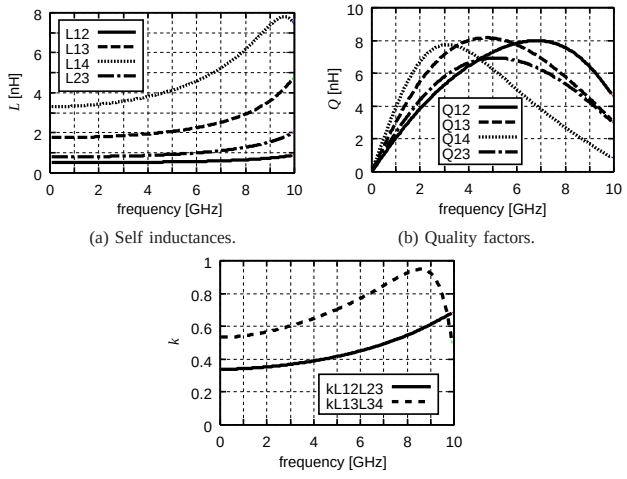
Fig. 3. Equivalent circuit of the 4-port inductor.

Figure 6 (a) shows the conversion gain and noise figure of the proposed mixer as functions of the RF frequency. Conversion gain is more than -10 dB at the RF frequency range from 1.5 to 6.0 GHz. The LO and RF signal amplitudes were set to be 7 and -20dBm, respectively. The IF frequency is 0.5 GHz. One of the IF outputs was terminated to 50 Ω load, and the other one was connected to the network analyzer (Agilent PNA E8364B). We measured the single-ended IF output, and used 3-dB correction factor to account for the 3-dB gain increase of the differential conversion gain. The measured NF is less than 15 dB at the frequcney range from 2.3 to 12 GHz. Figure 6 (b) shows the result of the two-tone test for the mixer at the RF frequency of 5.000 GHz, and the LO frequency of 4.500 GHz. As indicated in Fig. 6 (b), the proposed mixer circuit exhibited IIP3 of 13.6 dBm. Input signals of 5.000 and 5.005 GHz are utilized for two tone test. The measurement result of return loss at RF input port S_{RF} and IF output port S_{IF} are shown in Fig. 6 (c). As indicated in this figure, S_{RF} and S_{IF} exhibited a good response of less than -10 dB from 1.5 to 12 GHz.

Table I compares the performance of the proposed mixer circuit with that of previous work. The proposed mixer realizes the small area by using multi-port inductors.

IV. Conclusion

We proposed a novel small-area distributed mixer with multi-port inductors. This circuit accomplished wide range of the frequency down converting. Conversion gain of more than -10 dB, noise figure of less than 15 dB, return loss of less than -10 dB from 2.3 to 6.0 GHz, and IIP3 of 13.6 dBm are achieved. The proposed mixer is capable of realizing ultrawide-band RF receivers.



(a) Self inductances. (b) Quality factors.

(c) Coupling coefficients.

Fig. 4. Simulated characteristics of 4-port inductor.

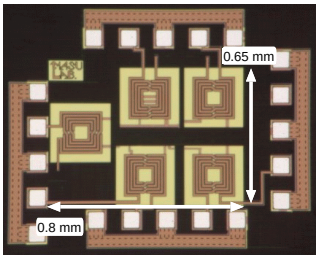
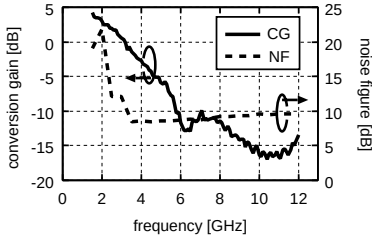
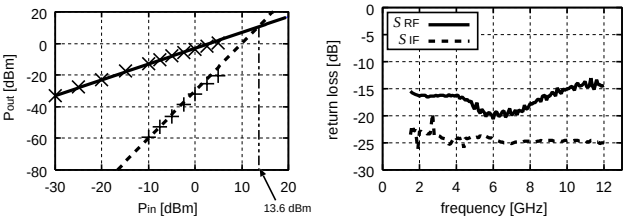


Fig. 5. Chip micrograph of fabricated novel small-area distributed mixer.



(a) Conversion gain and noise figure.



(b) Measured distortion. (c) Return loss at input and output ports.

Fig. 6. Measurements of the proposed mixer.

TABLE I
PERFORMANCE COMPARISON.

	RF(GHz)	conversion gain	power consumption	process	circuit area
[2]	3 - 8.72 GHz	3 dB	10.4 mW	0.18 μm CMOS	1.60 mm^2
[4]	3 - 22 GHz	3.6 dB	129.0 mW	0.18 μm CMOS	3.02 mm^2
[5]	1 - 14 GHz	1 dB	—	GaAs MESFET	2.70 mm^2
[6]	0.5 - 6 GHz	6 - 10 dB	1.0 mW	0.18 μm CMOS	4.9×10^{-3} mm^2
[7]	2.5 GHz	9 dB	2.8 mW	0.18 μm CMOS	0.03 mm^2
[8]	6 - 10.6 GHz	14 - 17 dB	0.2 mW	0.18 μm CMOS	0.73 mm^2
[9]	18 - 28 GHz	-2 - 0.7 dB	8.0 mW	130 nm CMOS	0.47 mm^2
[10]	0.3 - 25 GHz	11 dB	71.0 mW	0.18 μm CMOS	0.80 mm^2
this work	2.3 - 6.0 GHz	-2.2 dB	50.4 mW	0.18 μm CMOS	0.51 mm^2

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