A 1Tb/s 3W Inductive-Coupling Transceiver Chip

Noriyuki Miura and Tadahiro Kuroda
Keio University

Abstract– A 1Tb/s 3W inter-chip transceiver transmits clock and data by inductive coupling at a clock rate of 1GHz and data rate of 1Gb/s per channel. 1024 data transceivers are arranged with a pitch of 30μm in a layout area of 1mm^2. The total layout area including 16 clock transceivers is 2mm^2 in 0.18μm CMOS and the chip thickness is reduced to 10μm. Simple yet accurate model of inductive coupling is utilized for transceiver design. Bi-Phase Modulation (BPM) is employed for the data link to improve noise immunity, reducing power in the transceiver. 4-phase Time Division Multiplexing (TDM) reduces crosstalk and channel pitch. The BER is lower than 10^{-13} with 150ps timing margin.

I. Introduction

Performance gap between computation in a chip and communication between chips is widening. "System in a Package" (SiP) reduces distance between chips significantly, enabling a high-speed and low-power interface. An electrical non-contact interface using inductive coupling [1-3] has many advantages over mechanical interfaces [4,5] in terms of cost, scalability, reliability and flexibility. This paper presents the state-of-the-art inductive-coupling transceiver for over-Tb/s data communications.

II. Chip Design and Measurement Results

Figure 1 presents the block diagram of the inductive-coupling transceiver. The transceiver comprises of 16 slices of 64ch block. Each of 64ch blocks consists of 64 data transceivers and one clock transceiver. Clock of the transmitter *Txclk* is transmitted through the inductive coupling and clock of the receiver *Rxclk* is recovered by the clock transceiver. The clock frequency is 1GHz. Phase Interpolator (PI) generates 4 time slots in one clock cycle by creating 4-phase clocks from both *Txclk* and *Rxclk* for Time Division Multiplexing (TDM). Data transceivers are divided into the time slots to reduce the crosstalk. Each data transceiver communicates at 1Gb/s/channel. 1Tb/s data bandwidth is obtained by 1024 parallel data links.

Figure 2 shows microphotographs of the test chips fabricated in 0.18μm CMOS. The transmitter chip is placed on top of the receiver chip, as both chips in face up. Both chips are polished to 10μm thickness. Communication distance including an adhesive layer is 15μm. The clock transceiver transmits 1GHz clock by the inductor with a diameter of 200μm. The clock transceiver is set up for every 64 data transceivers. The data transceiver communicates at 1Gb/s/channel by the inductor with a diameter of 29.5μm. 1024 data transceivers are arranged with a pitch of 30μm.

The inductive coupling is designed based on equivalent circuits [6] shown in Fig.3.(a). The inductive coupling functions as a differentiator ($j\omega M$). Self inductance and parasitic capacitance of the metal inductor limit bandwidth up to self-resonant frequency, f_{SR}. For the data link, pulse signal is transmitted so that f_{SR} should be twice higher than 1/pulse-width. For the clock link, f_{SR} is set to 1GHz with higher Q to cut ambient noise. Figure 4 summarizes optimal layout and circuit parameters for the data and clock links.

Measurement results of the clock transceiver are depicted in Figure 5. 1GHz clock is successfully transmitted. Rms jitter is 9.5ps in *Rxclk*, some of which is caused by 6ps jitter in *Txclk* by an external clock generator. The clock transmitter consumes 4mW and the clock receiver consumes 6mW from 1.8V supply.

Figure 6 shows the schematic diagram of the data transceiver and simulated waveforms. Bi-Phase Modulation (BPM) signaling is employed for the data link. In every clock cycle, an H-bridge circuit in the data transmitter generates positive or negative pulse current, I_T, according to *Txdata*. A sense-amplifier flip-flop in the data receiver samples positive or negative pulse voltage, V_R, corresponding to the polarity of I_T, and then it recovers *Rxdata*. Unlike with Non-Return-to-Zero (NRZ) transceiver [1,2], the BPM transceiver always generates V_R signal in every clock cycle. Therefore noise immunity of the receiver is improved and receiver's sensitivity in the BPM signaling can be maximized while that in the NRZ signaling has to be set low enough to ignore crosstalk. The high sensitivity in the BPM signaling enables lower BER with smaller transmission power. A snapshot of data waveforms in Fig.6 shows successful 1Gb/s data communications with 2^{23}-1 Pseudo Random Binary Sequence (PRBS). Measured BER is lower than 10^{-13} with transmission power of only 2mW.

Measured timing bathtub curve is shown in Fig.7. BER lower than 10^{-13} is examined by the 2^{23}-1 PRBS data of 1Gb/s. Timing margin of 150ps is obtained. The margin is sufficiently wide so that the timing can be easily designed against jitter, skew and PVT variations.

BER dependence on channel pitch and the number of phases in TDM was measured. The measured results are plotted in Fig.8. By increasing the number of phases in TDM, crosstalk is reduced and the channel pitch can be shortened for the same BER. 1024 transceivers arranged with a pitch of 30μm operate at BER lower than 10^{-13} with the 4-phase TDM. As a result, aggregate data bandwidth of 1Tb/s is achieved with 1mm^2 area for the data transceivers.

III. Summary

Chip performance is summarized in Fig.9 and compared with transceiver presented at ISSCC past ten years ('96~'05). The highest 1Tb/s data bandwidth is obtained by 1024 data transceivers arranged with a pitch of 30μm. The bandwidth is 3.3 times higher than Rambus FlexIO implemented in CELL processor [7]. 1GHz clock is also provided by the inductive coupling. The transceiver chip consumes 3W from 1.8V supply where data transceivers consume 2.4W, clock transceivers and phase interpolators consume 0.6W. The layout area for the data link is 1mm^2 and that for the clock link is 1mm^2 in 0.18μm CMOS. Power/bandwidth is the lowest 3mW/Gb/s that is 7 times lower than [7] and area/bandwidth is the smallest 1mm^2/Tb/s that is 4 times smaller than [7] even in less advanced technologies.

Acknowledgements

The authors are grateful to Prof. Takayasu Sakurai with the Univ. of Tokyo and Masamoto Tago, Muneo Fukaishi, and Yoshihiro Nakagawa with NEC Corporation for their valuable assistance in measurement and fruitful discussion. The VLSI chips in this study have been fabricated in the chip fabrication program of VDEC, the University of Tokyo in collaboration with MOSIS and TSMC.

References

[1] D. Mizoguchi, *et al.*, *IEEE ISSCC Dig. Tech. Papers*, pp.142-143, Feb. 2004.
[2] N. Miura, *et al.*, *IEEE J. Solid-State Circuits*, vol.41, no.1, pp.23-34, Jan. 2006.
[3] N. Miura, *et al.*, *IEEE ISSCC Dig Tech. Papers*, pp.424-425, Feb. 2006.
[4] T. Ezaki, *et al.*, *IEEE ISSCC Dig. Tech. Papers*, pp.140-141, Feb. 2004.
[5] J. Burns, *et al.*, *IEEE ISSCC Dig. Tech. Papers*, pp.268-269, Feb. 2001.
[6] N. Miura, *et al.*, submitted to *IEEE J. Solid-State Circuits*.
[7] K. Chang, *et al.*, *IEEE ISSCC Dig. Tech. Papers*, pp.526-527, Feb. 2005.

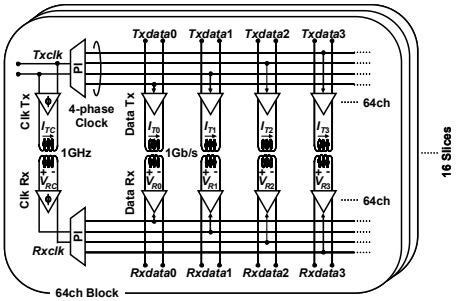


Fig.1 Block diagram of inductive-coupling transceiver.

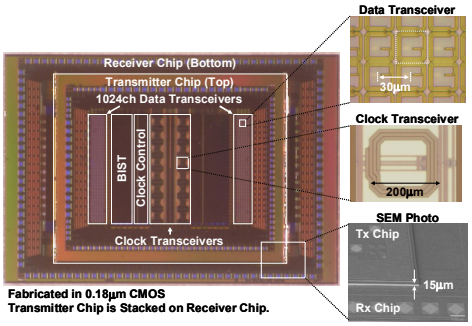


Fig.2 Chip microphotographs of inductive-coupling transceiver.

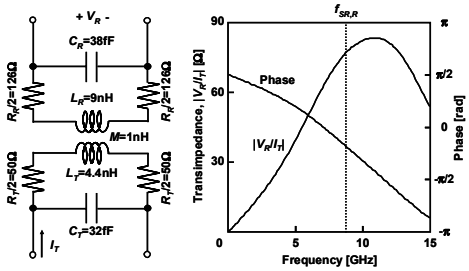
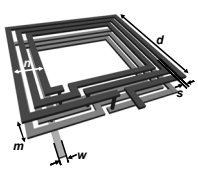


Fig3 Model of inductive coupling (with circuit parameters for the data link).



Parameter	Data Link		Clock Link
	Tx	Rx	
Diameter, *d*	29.5μm	29.5μm	200μm
Wire Width, *w*	1μm	0.5μm	10μm
Wire Space, *s*	0.5μm	0.5μm	1μm
Turns, *n*	3	4	3
Layers, *m*	4	4	4
L	4.4nH	9nH	30.6nH
C	32fF	38fF	484fF
R	100Ω	252Ω	44Ω
f_{SR}	13.4GHz	8.6GHz	~1GHz
M	1nH		22nH

for Channel Pitch=30μm, Communication Distance=15μm in 0.18μm CMOS

Fig.4 Layout and circuit parameters of inductive coupling.

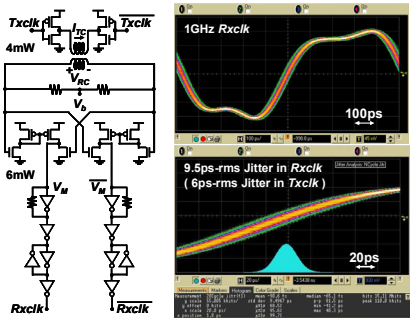


Fig.5 Wireless clock transceiver and measured received clock and jitter.

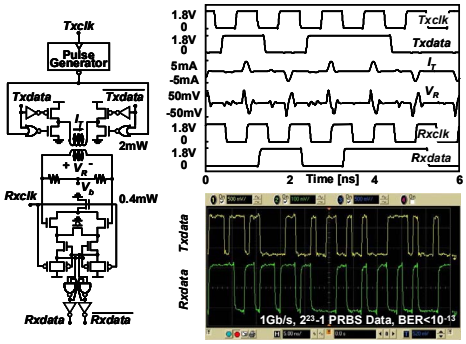


Fig.6 BPM data transceiver, simulated waveforms and snapshot of data waveforms.

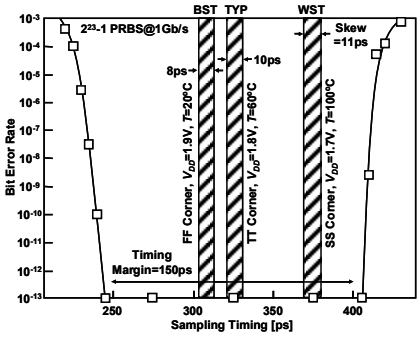


Fig.7 Measured timing bathtub curve.

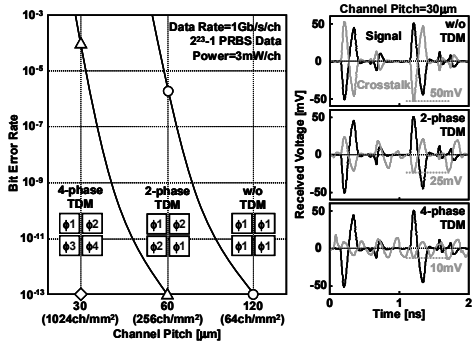


Fig.8 Measured BER dependence on channel pitch.

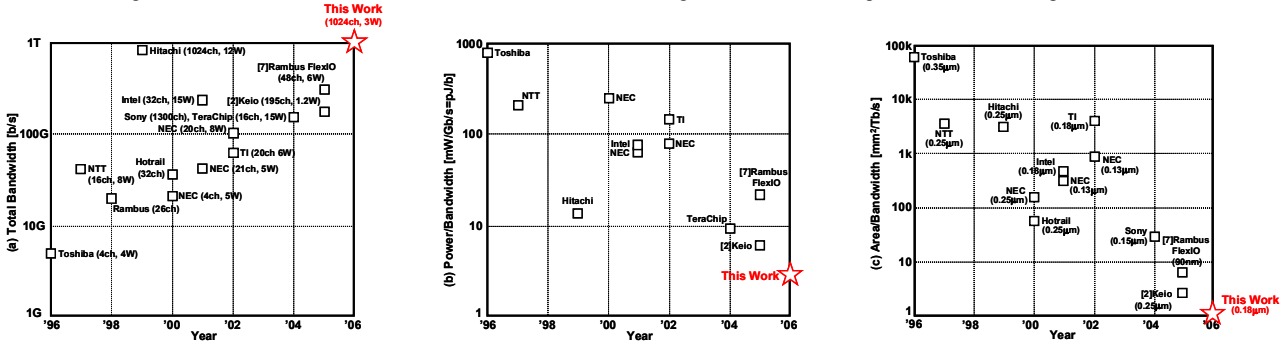


Fig.9 Performance of ISSCC transceiver in terms of (a) total bandwidth, (b) power/bandwidth and (c) area/bandwidth.