

# Preferable Improvements and Changes to FB-DiMM High-Speed Channel for 9.6Gbps Operation

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**Abstract** - In this paper we showed the signal degradation parts in High-speed channel of FB-DiMM system. And we also showed possible countermeasure. For the verification propose and also for establishing the precise modeling and simulation method, we compared measurement and simulation up to 9.6Gbps operation with test board. And we get good relation between them. After getting the calculated loss budget of estimated system, we made recommendations of preferable changes to Main board and DiMM socket.

## I. Introduction

Fully Buffered DiMM (FB-DiMM) is the new type of DiMM, which introduced from DDR2. In FB-DiMM system shown in Fig.1, Controller communicates with Advanced Memory Buffer (AMB) of each DiMM using differential signal. And AMB manages the entire DRAM in DiMM using Single-end signal.

From the first time, we feel the difficulty in differential High-speed channel especially when we use the DDR3 Frequency range. DDR3 data rate available up to 1.6Gbps and FB-DiMM specification of DRAM interface to differential High-speed channel gear ratio is set to 6. This mean high-speed channel have to be feasible up to 9.6Gbps. From the preliminary transient simulation, we noticed the eye waveform at the receiver is very bad in 9.6Gbps operation. So

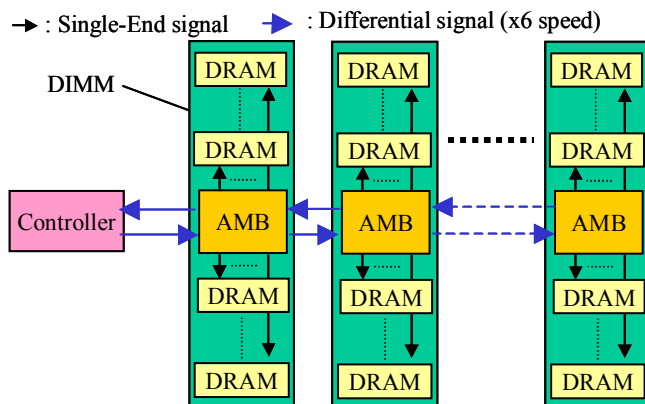


Fig. 1. Illustration of FB-DiMM system

from the infrastructure point of view, we feel the emerging possibility of changes to DiMM socket and Main board material in the 9.6Gbps operation range.

Another suspicion was the accuracy of preliminary transient simulation. We suspect not only electrical model of each parts, but also the simulator itself. So we started to build the experimental board. The target of this board is to estimate insertion loss of the target system and correlate the data with simulation. Object of this report is verification of 9.6Gbps operation with existing system and to make possible recommendations to Main board, DiMM socket, and DiMM.

## II. Expected Loss and improvement method in each part

### 1. Connector

Commonly used through hole type connector case, this through hole under connector is the measure impedance mismatch point.

Through hole under connector is too capacitive because the pin of connector inserted in large through hole, which capacitive coupled with other layer of main board. So, this through hole is relatively low impedance and generate impedance mismatch. And this through hole has another serious structure problem that behave like open stub when signals routed in surface layer of main board.

Fig. 2 shows the two distinct type of connector Illustration for connecting scheme. One is through hole type connector and the other is ball grid array (BGA) type surface mount connector. In these cases, top surface layer of main board is used and connect to DiMM surface layer. Fig. 2 also shows the s-parameter measurement result of each case. Over 6GHz frequency range, reflection and insertion loss grow extremely bad in through hole type connector case. But BGA type connector's s-parameter result shows small transmission loss and impedance mismatch can be minimized.

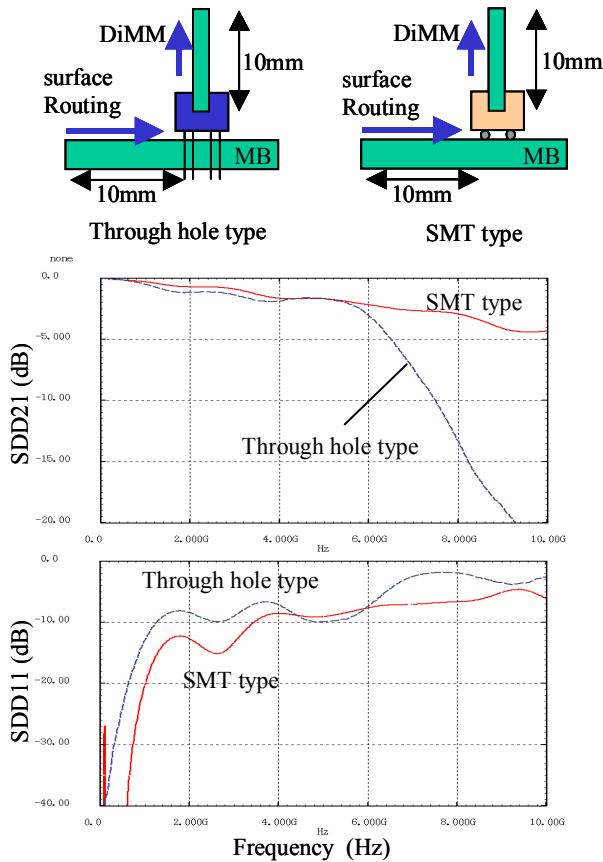


Fig. 2. Illustration of 2 different type connector and Measured S-parameter

2. DiMM edge finger

DiMM edge finger part is relatively large area that is capacitive coupled with DiMM internal VSS layer. And this excessive capacitance make the impedance mismatch. Fig. 3 shows Layout of DiMM edge finger part and measured s-parameter. Layout case (b) is the countermeasure to improve the impedance mismatch in this edge finger part.

3. Transmission line

Preliminary estimation of loss budgets calculation, loss in transmission line is the biggest part of all. So, we prepared the test board with 3 board materials. One is usual FR-4 and 2nd. is Halogen free FR-4 and 3rd. is low transmission loss material. Fig. 4-a shows the cross section and measured dimension of each case. Fig. 4-b shows comparison of measured transmission loss/m for above 3 materials with strip line and micro strip line case. Lower transmission loss in micro strip line rather than strip line is observed when using high dissipation factor material like FR-4. But low loss material case, strip line brings lower transmission loss. Reason of this loss reversal is

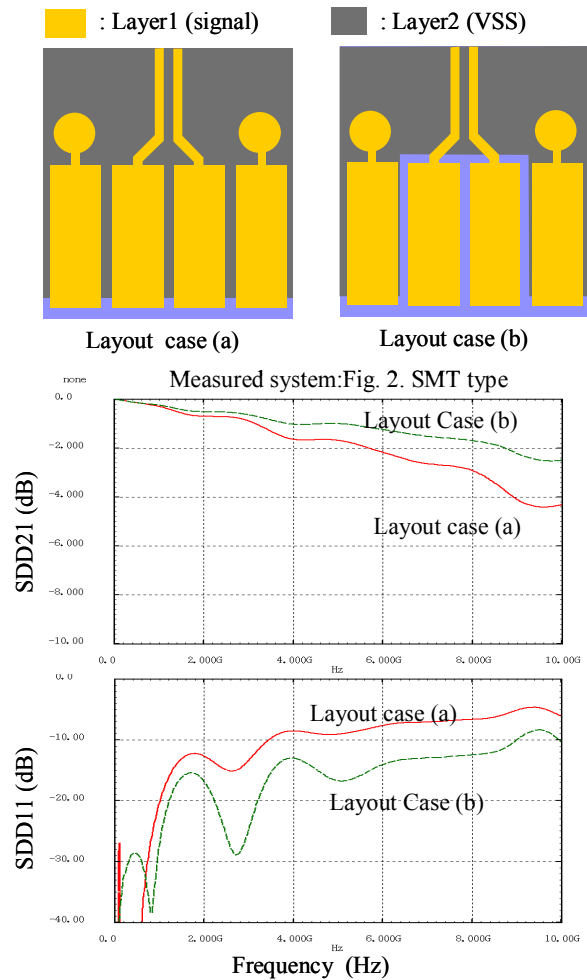


Fig. 3. Layout of DiMM edge finger part and measured s-parameter

existence of solder resist in micro strip line. And we have to mind that the shape and thickness of solder resist is not so well controlled because of formation methodology limitation.

4. Through via

Via case is almost the same situation as through hole under connector. Lower impedance and the stub effect is also the serious problem. Fig. 5 show the two distinct types through hole connection and modeled s-parameter. Connection from top layer to bottom layer case shows smaller loss than connection from internal to bottom layer case. The difference of this case is stub structure. Board assumption of these cases is 1.5mm thick 8layer. If board thickness bigger than 1.5mm, through via stub bring even bad result. There are several ways to avoid this stub structure like build up board or counter drilling of via.

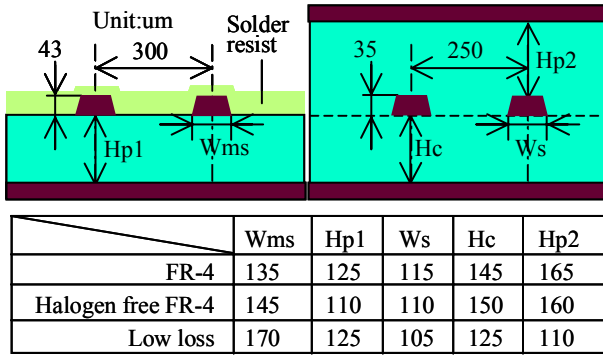


Fig. 4-a. Measured cross section Dimension of transmission line

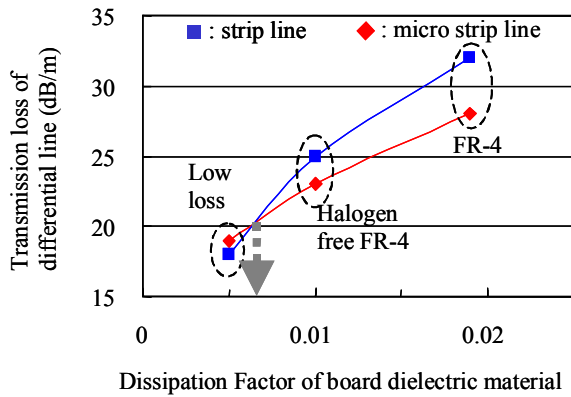


Fig. 4-b. Measured transmission loss of main board using 3 different dielectric material

### III. Verification

#### 1. S-parameter modeling vs. Measurement

We made test board and measured the s-parameter up to 10GHz. An example of test board Illustration is shown in Fig. 6-a. On the other hand, we tried to make the electrical model of every parts of this Test board. At first, we modeled the transmission line with 2D-EM solver program. But, the modeled s-parameter was not so well fitted to measured s-parameters especially the micro strip line case. We finally used 3D-EM solver program not only DiMM socket but also in transmission line. To differentiate from the accidental well-fitted result, we compared modeling and measurement in five different conditions including the combination of connector structure and transmission line structure. Fig. 6-b shows an example of s-parameter comparison of electrical modeling and measurement result. In s-parameter up to 10GHz, modeling and measurement fit well enough in all five conditions.

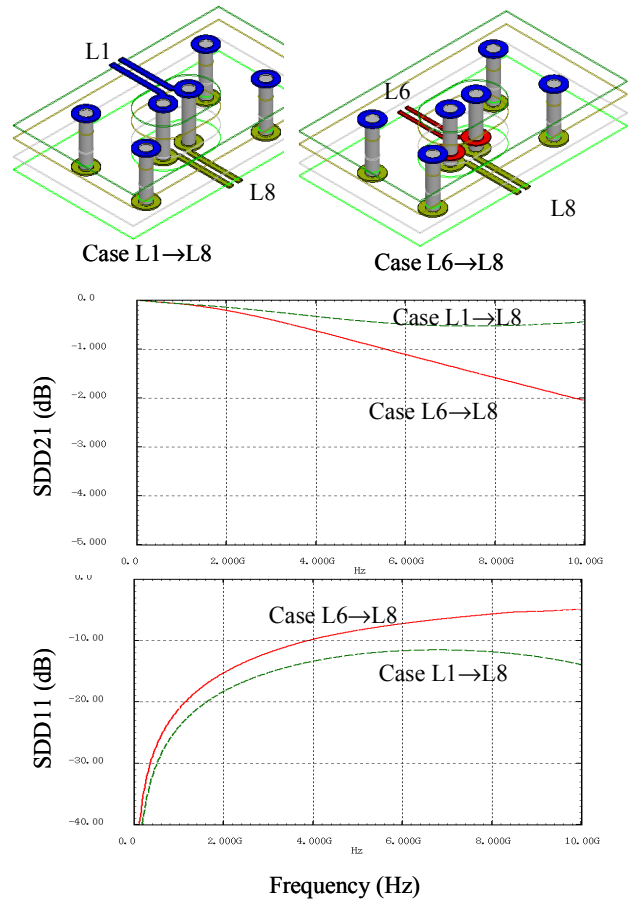


Fig. 5. Layout of two distinct through hole connection and modeled s-parameter

#### 2. Transient waveform simulation vs. Measurement

We tried transient waveform simulation in two ways. First way is using the measured s-parameter model directory in transient simulation. Another more realistic way to adopt for the system variation is using the combination of each part model. In anyway, when we simulate lossy system and data rate over few Gbps, not all the transient simulator output the same waveform result, even if we input the same simulating conditions. But, this situation is gradually getting better recently. Selecting the simulator and method, we can get fairly good relation between transient simulation and measured waveform. To differentiate from the accidental well-fitted result, we compared simulation and measurement in five different conditions that was used in previous s-parameter case. Fig. 6-c shows the example comparison of simulated and measured waveform with pseudo-random bit pattern of 10Gbps operation. In all five conditions, simulated waveforms almost match with the measurement result.

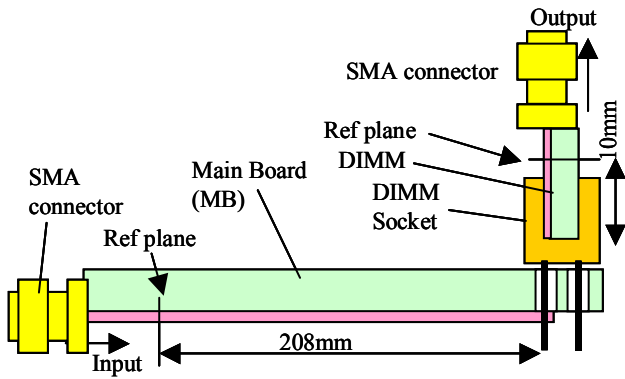


Fig. 6-a. Illustration of Test board example for verification

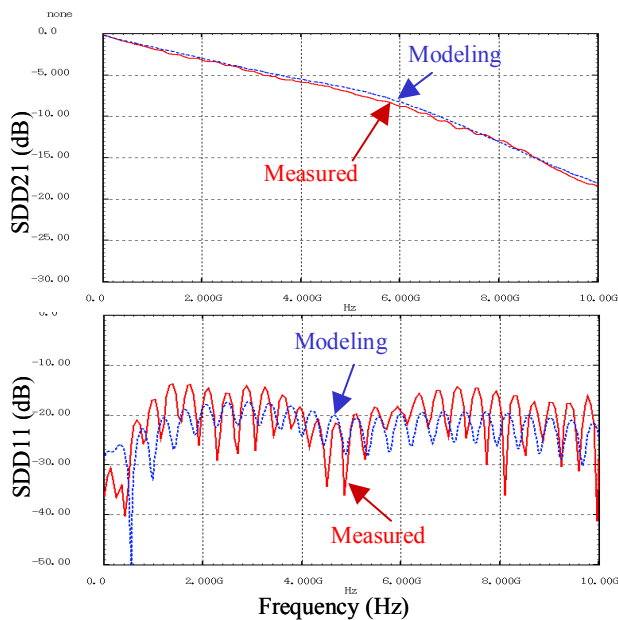


Fig. 6-b. Example of Measured S-parameter and Simulation result (Fig. 6-a. structure case)

IV. Conductance loss estimation

We carefully set the target loss maximum from driver PKG ball to receiver PKG ball as 14.5dB. And we accumulated the total conductance loss using measured loss of micro strip and strip line, loss by main board via, loss by connector, loss by TH stub under connector, and estimated the total loss in Fig. 7-b. System assumption in this calculation is illustrated in Fig. 7-a. In this calculation, conventional type infrastructure of through hole type connector and FR4 motherboard seems to be feasible up to 10Gbps. But it seems, BGA type connector and Halogen free FR-4 are recommended for getting better loss margin.

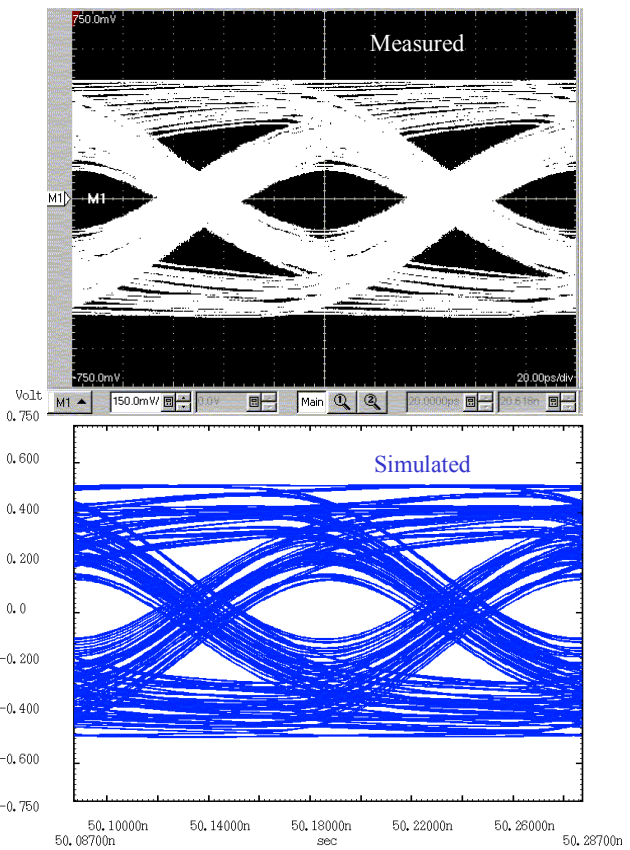


Fig. 6-c. Example of 10Gbps\* Measured Eye pattern and Simulation result (Fig. 6-a. structure case)

\*: Pseudorandom bit pattern without de-emphasis

V. Conclusion

We verified 9.6Gbps signal transmission of FB-DiMM differential high-speed channel using test board measurement result. We calculated the voltage loss of each parts using measurement result. And judged that, conventional FR-4 main board and through hole type DiMM socket can accommodate up to 9.6Gbps operation. However, transmission loss by through hole stub under connector and long line length in main board is critically big. So, we recommend the below changes.

1. The change around connector that include changing the connector structure like surface mounts type.
2. The change to lower dielectric loss material than usual FR-4 for main board. Halogen free FR-4 seems to be a suitable choice.

Acknowledgement

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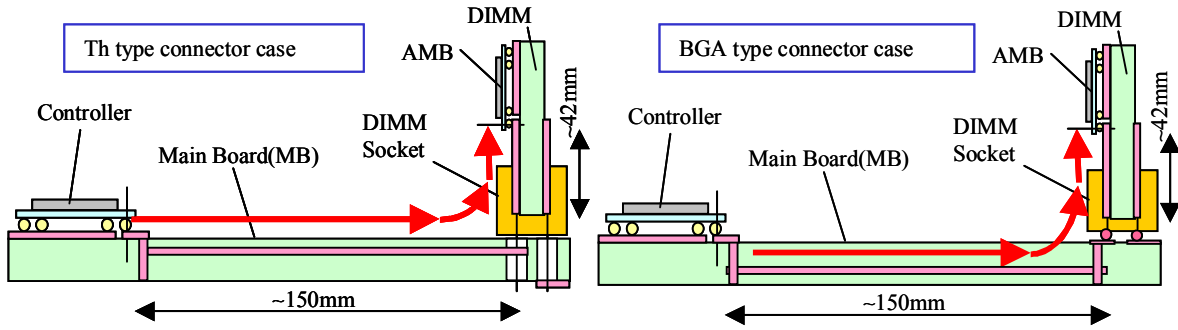


Fig. 7-a. Illustration of FB-DiMM High-speed channel for Loss budget calculation

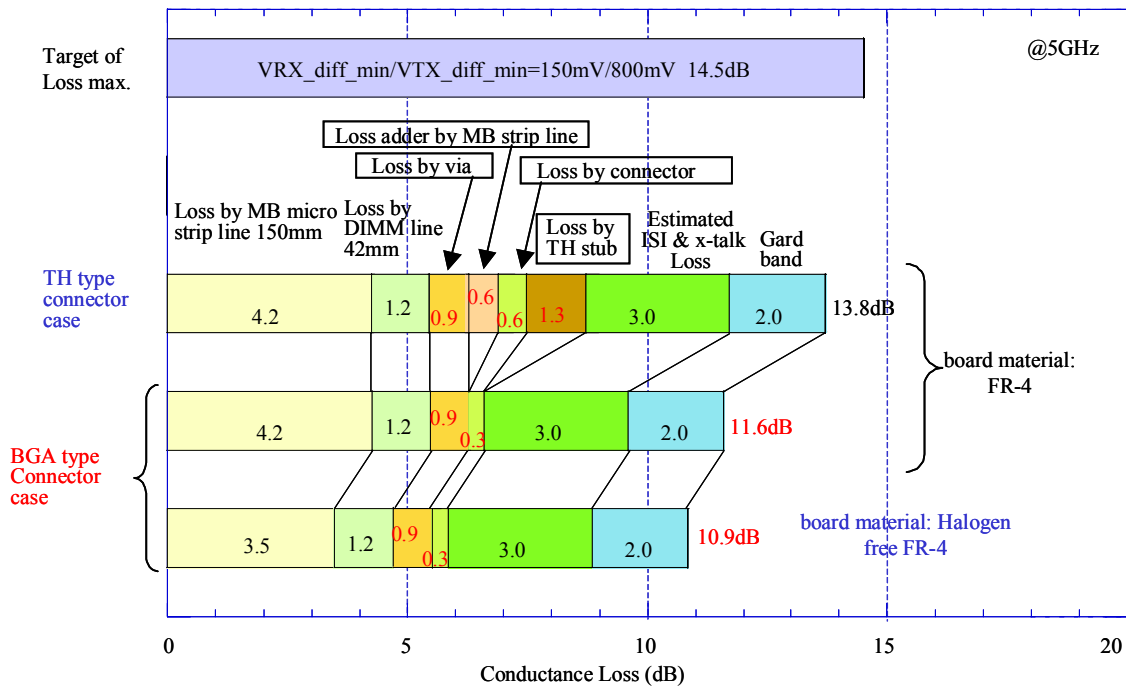


Fig. 7-b. Connector type and comparison of total Conductance Loss (DiMM to Controller case estimation)