Warning: Launch off Shift Tests for Delay Faults May Contribute to Test Escapes

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Abstract - Two methods to apply tests to detect delay faults in standard scan designs are used. One is called launch off capture and the other is called launch off shift. Launch off shift test method has the advantage that it provides higher fault coverage at reduced test generation time and test pattern counts. However a concern expressed often in the literature is the potential over testing or yield loss caused by the fact that launch off shift operates the circuit under test in non-functional manner. In this paper we present data, for the first time, which points to another potential problem with launch off shift tests. The data presented for ISCAS-89 benchmark circuits shows that a considerable numbers of functionally detectable transition delay faults are not detected by the normally used launch off shift tests that use a single fault activation cycle. Functionally detectable faults that escape tests could cause circuit malfunction in normal operation. Thus launch off shift tests when used in manufacturing test may result in test escapes. We also present data that shows that if launch off shift tests with multiple fault activation cycles are used essentially all functionally detectable faults can be detected.

I. Introduction

As the density and complexity of VLSI circuits increase, tests for manufactured devices based on stuck-at fault model are becoming less effective in detecting defects that are typically resistive opens and shorts. To achieve low DPM (defective parts per million shipped parts) tests for delay faults, transition delay faults (TDFs) are becoming an essential part of manufacturing test to ensure high quality of shipped products. However, there are conflicting concerns regarding the use of tests for delay faults. These concerns are related to tests using scan which is essentially the only practical method for testing manufactured circuits. These conflicting concerns can be simply stated as under testing and over testing or overkill. Under testing manufactured devices cause test escapes. That is, some defective devices may pass tests applied. Over testing is said to occur when a device that can function correctly fails manufacturing tests thus reducing yield.

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In standard scan designs, delay faults are tested using skewed-load tests, also called launch off shift (LOS) tests [1], or using broadside tests, also called launch off capture (LOC) tests [2]. These test methods may not detect all the detectable TDFs. Scan designs using scan cells with three latches [3], called enhanced scan designs, permit the application of arbitrary two-pattern tests. In such designs all the detectable TDFs can be detected. Enhanced scan may not be suitable for many designs due to its larger area overhead. Results on industrial designs show that LOS tests achieve higher TDF coverage than LOC tests. Further more both the test generation effort or run time and the number of tests using LOS tests are much smaller [4]. However, the often mentioned concern with LOS tests is that they may lead to over testing and hence cause yield loss [5]. This is due to the fact that LOS tests achieve higher fault coverage than is possible using functional operation of the circuit [5].

In this paper we investigate the complimentary issue of whether LOS tests do not detect some functionally detectable faults and the extent of this problem. Functionally detectable faults could cause circuits to malfunction in normal operation. Thus this study establishes, for the first time, the potential under testing by LOS tests that could cause test escapes in shipped products.

The remainder of the paper is organized as follows. In Section 2 we discuss test application methods for delay faults in circuits using standard scan and earlier related works on which the work presented in this paper is based. In Section 3 present the test generation procedures used in this work. In Section 4 experimental results are presented and Section 5 concludes the paper.

2. Preliminaries

In this section we review known methods to test for delay faults in standard scan designs. Since our focus in this paper is transition delay faults, all discussions assume TDFs.

2.1 Tests for TDFs in standard scan design

The set of TDFs contains two faults for each circuit line. One is the slow to rise (STR) fault and the other is

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the slow to fall (STF) fault. For standard scan design illustrated in Figure 1 two methods have been used to detect TDFs. One is called the launch off capture and the other is called the launch off shift. Both methods use a two pattern test <V1, V2> to detect a targeted fault. In both methods, the first pattern V1, called the initialization pattern, is scanned in, with the scan enable (SE) signal asserted. For a slow to rise (slow to fall) TDF, V1 sets the fault site to 0(1). The second pattern V2 is generated differently in the two methods. In LOC the second pattern is generated through the combinational logic of the circuit under test (CUT) by applying a clock pulse with SE de-asserted. This is referred to as the launch cycle and is illustrated in Figure 2(a) for a scan chain of length *n*. Application of V2 activates the fault by launching a transition at the fault site and also propagates the fault effect to an observed output (primary output or a scan cell). For a slow to rise (slow to fall) TDF V2 is a test for a stuck-at-0 (stuck-at-1) fault at the fault site. Following the application of V2, another clock pulse is applied with SE still de-asserted to capture the CUT response to the test. This is also shown in Figure 2(a) where the corresponding clock pulse is labeled *C* for capture. Often the two clock pulses used to launch a transition and capture test responses are both called capture cycles. Thus a standard LOC test uses two capture cycles. For LOS tests V2 is derived from the scanned in V1 by shifting the scan chain by one position with SE asserted and then applying another clock cycle with SE de-asserted to capture the CUT response to the test. The timing diagram for LOS tests is shown in Figure 2(b). Thus in both LOC and LOS tests, two test cycles are used. In this work we refer to the second test cycle as the test response capture cycle and the first test cycle as the fault activation cycle. It should be pointed out that a variation on the LOS tests as described above is also used in which the last shift (the *nth* shift for a scan chain of length *n*) is used to launch V2.

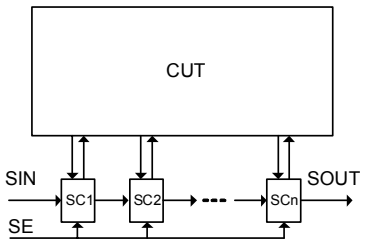

Figure 1: Standard scan

Since V2 is correlated to V1, in both the LOC and the LOS tests due to the manner in which it is derived, transition delay faults at some fault sites may not be detected by these test methods but are detected if enhanced scan is used. Even though both LOC and LOS test methods do not detect transition faults at some fault sites experimental results on industrial as well as benchmark circuits have shown that LOS test method achieves higher TDF coverage than LOC tests. However since the second pattern V2 of a two pattern test is derived through a shift of the first pattern V1 LOS tests tend to operate the circuit in non-functional operation and cause over testing [4]. In LOC tests the second pattern of a two pattern test is derived through functional logic of the circuit under test and thus the over testing by LOC tests is expected to be less. One could reduce over testing using the following strategy [6]. Determine the faults that are not detectable by functional tests and avoid their detection by masking the outputs to which the functionally untestbale fault effects are propagated. Other approaches to reduce/eliminate over testing are discussed in the next section.

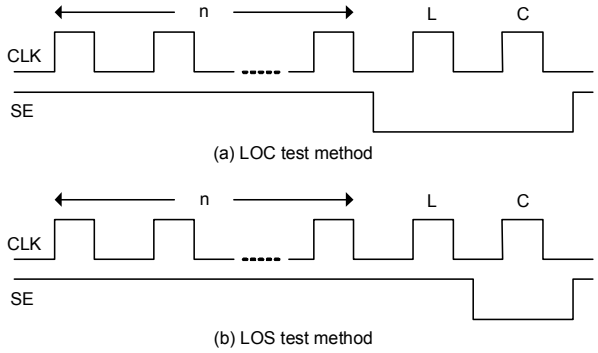

Figure 2: Timing diagram for LOC and LOS test methods

Our focus in this work is the issue of under testing. By under testing we mean the faults that are not detected by LOS tests but effect functional operation of the circuit.

2.2 Pseudo-functional tests for TDFs

As noted above over testing in scan based test is caused by non-functional operation during test. One way to avoid non-functional operation during test is to use LOC tests together with the condition that the scanned in first pattern V1 of a two pattern test is a reachable state [7, 8]. However determining that a state is reachable for large designs may not be feasible. For this reason an alternate approach is to use tests that avoid using un-reachable (also called illegal states) during test [9-11]. In this approach the illegal states for a circuit under test are determined and the scanned in state for the first pattern V1 of a two pattern LOC test is chosen such that it is not one of identified illegal states. Such tests are called pseudo-functional tests [10]. The reason for calling them pseudo-functional is that not all illegal states are identified by the procedures used. Recent work on improved methods to identify illegal states of a sequential circuit have lead to pseudo-functional tests that avoid detection of all known functionally untestable transition

faults [11]. The method in [11] derives pseudo-functional LOC tests that use a single fault activation cycle (launch cycle). However, recently it has been shown that in standard scan designs at some fault sites TDFs can only be detected by using multiple activation cycles [12, 13].

In the work presented in this paper we extend the method in [12] to derive pseudo-functional tests that use multiple fault activation cycles to obtain the set of TDFs that can be detected using pseudo-functional tests. We use this set of faults to determine the extent of under testing that may occur using standard LOS tests that use a single fault activation cycle. We also investigate how under testing by LOS tests can be remedied.

2.3 Multiple fault activation cycle tests

For the sake of completeness we include the examples from [12] to demonstrate the need for considering multiple fault activation cycles to detect TDFs at some fault sites. Consider the sequential circuit shown in Figure 3. Assume a slow to rise (STR) TDF on line *a1*. By definition a transition fault represents a delay fault of large (infinite) size. Consider a sequence of inputs 011 applied to *a* in three consecutive clock cycles. The values on all the signal lines in the circuit are shown using the standard notation of p/q to represent fault-free/faulty values on a signal line. It can be seen that the TDF on *a1* affects the circuit performance in the sense that in its presence the circuit malfunctions when the input sequence 011 is applied.

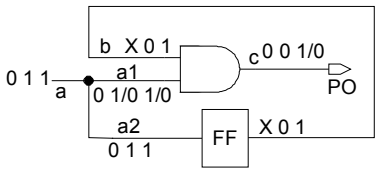

Figure 3: A sequential circuit with STR fault at *a1*

Now consider generating a test to detect the STR fault on *a1* using a standard LOC test that uses a single fault activation cycle. This is illustrated in Figure 4(a) where an ILA (iterative logic array) of two time frames is shown. Clearly the STR fault at *a1* is not detectable since the fault effect is not propagated to PO or to FF. Next consider a LOC test that uses two cycles for fault activation followed by a capture cycle. Such a three cycles test, which uses an ILA of three time frames, is illustrated in Figure 4(b). Using a three cycle test the STR fault on *a1* is detected as shown by the 1/0 on output *c* in time frame 3. The example above shows that TDFs at some fault sites may not be detectable using LOC tests that use only one fault activation cycle but may be detectable using tests with more than one fault activation cycles. As illustrated below similar situations may occur when LOS tests are used.

For the circuit shown in Figure 5(a) assume a slow to

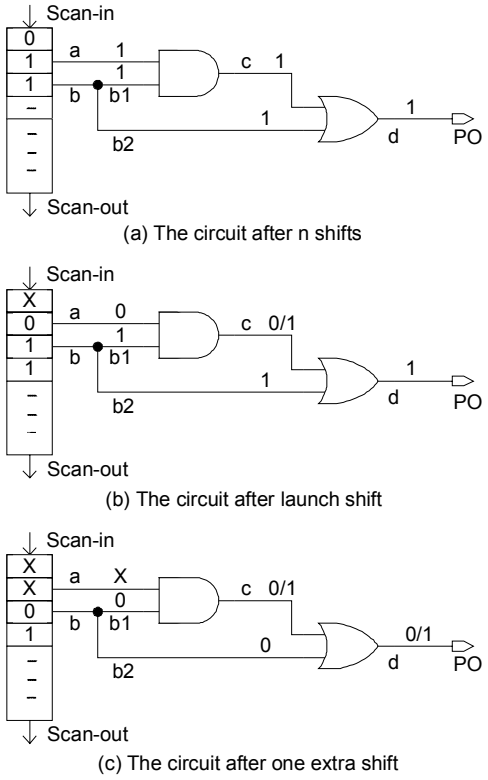

Figure 5: LOS test for a STF fault at *c*

fall (STF) fault on line *c*. This fault cannot be detected using a standard LOS test that uses two test cycles as illustrated in Figure 5(b). However, it can be detected by using a three cycle LOS test as shown in Figure 5(c). In applying a three cycle LOS test, after V1 is scanned in one uses two additional shifts of the scan chain to activate the fault, followed by one clock pulse applied with scan enable inactive to capture the test response.

The examples given above illustrate that the LOC and LOS tests using two test cycles may not detect TDFs at some fault sites that affect circuit operation. Faults at such sites affect circuit operation when the size of the delay fault at these sites is sufficiently large. TDFs at such fault

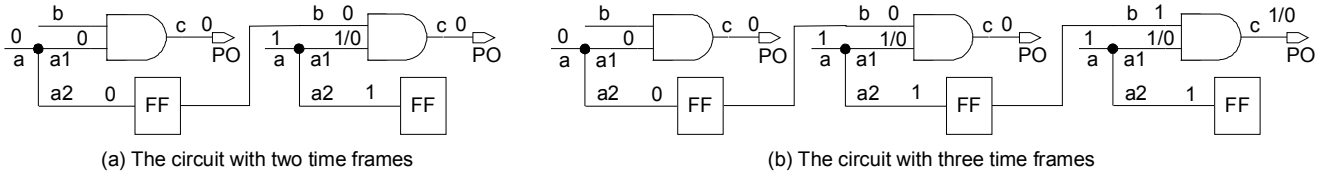

Figure 4: LOC test for the circuit in Figure 3

sites may be detected by using LOC and/or LOS tests using multiple cycles to activate the faults.

It is important to point out that earlier, Cheng [14] had investigated detection of TDFs of different sizes in synchronous sequential circuits without scan. In [14] fault simulation to determine the ranges of delay fault sizes detected by a given test sequence and generation of tests for transition faults in sequential circuits was investigated. Tests for scan designs were not considered in [14].

3. Pseudo-functionally detectable TDFs

In order to determine the extent of under testing by LOS tests for TDFs we first need to determine the set of all pseudo-functionally detectable TDFs followed by determining the number of pseudo-functionally detectable faults that are not detected by LOS tests. To determine all pseudo-functionally detectable TDFs we extended the method of [11] to derive tests that use multiple fault activation cycles. The steps of this procedure are given next.

We implemented an ATPG to generate pseudo-functional LOC tests for TDFs using multiple activation cycles. The ATPG uses two procedures. The first procedure determines illegal state cubes using static learning as discussed in [11]. Each illegal state cube we retain has at most three specified state variables and the remaining state variables are unspecified. For example consider a circuit with six state variables, s1, s2, s3, s4, s5 and s6. An illegal state cube could be 0X1XX1. An illegal state cube can be regarded as a product of state variables. For example the state cube 0X1XX1 can be regarded as the product s1's3 s6. We construct a circuit which has one AND gate for each product term representing an illegal state and an OR gate that realizes the OR of all AND gates. We call this circuit ISC (for illegal state circuit) and append ISC to the circuit under test for which we generate tests. Note that ISC can be factored to obtain a simpler circuit. In the second procedure we determine all pseudo-functionally testable faults in the circuit under test using tests with multiple fault activation cycles.

The procedure described above finds all pseudo-functionally detectable faults using 1, 2, …, up to (*ILA_limit-1*) fault activation cycles.

We also implemented a LOS test generation procedure for TDFs that uses multiple fault activation cycles. This procedure uses essentially all the steps in the procedure above except that it does not use the illegal state information and hence the circuit ISC to restrict the tests generated. The other difference is that LOS tests instead of LOC tests are generated. Thus the procedure finds all faults that are detectable by LOS tests with up to (*ILA_limit-1*) fault activation cycles.

Procedure_Pseudo functionally_detectable_faults

1. Let C be the circuit under test and ISC be the circuit obtained by the procedure described above.
2. Set m = 2; Initialize *UF* to include all the TDFs in C;
3. Construct an iterative logic array (ILA) of C with length equal to m and add the circuit ISC in the first time frame of the ILA;
4. For each STR (STF) fault f in *UF*, inject a stuck-at-0(1) fault in the last time frame.
5. Combinational ATPG is performed with the following conditions:
   - (i) the fault site is set to 0(1) in the first time frame and the fault sites in the last (m-1) time frames are set to 1(0) simultaneously
   - (ii) the output of the ISC circuit is not set to 1 (this precludes the scanned in state of the test from being an illegal state);
6. If a test t is found for f, fault simulate t on all the faults in *UF*, using the current test criteria, and remove the detected faults from *UF*;
7. After targeting all the faults in *UF*, report the set of faults detected using (m-1) fault activation cycles;
8. Set $m = m+1$; If $m \leq ILA\_limit$, go to step 2.

4. Experimental results

We implemented the procedures to determine TDFs that are detectable by pseudo-functional tests that use multiple fault activation cycles as well TDFs that can be detected by LOS tests that also use multiple fault activation cycles. We applied these procedures to ISCAS-89 benchmark circuits. Results of these experiments are given in Tables 1 through 3.

In Table 1 after the circuit name we give the total number of TDFs. Next the numbers of faults detected by pseudo-functional (PFN) tests using up to 11 fault activation cycles, and the numbers of faults detected by the normally used LOS tests with a single fault activation cycle. Next we give the number of TDFs which are detected by pseudo-functional tests but are not detected by the LOS tests. The faults not detected by LOS tests as a percentage of the number of faults detected by PFN tests are given in the last column. In the last row we give the average of the percentage of faults not detected by the

LOS tests. From Table 1 it can be seen that as expected the numbers of faults detected by LOS tests are higher even though they use a single fault activation cycle and the pseudo-functional tests use up to 11 fault activation cycles. At the same time substantial numbers of pseudo-functionally detectable faults are not detectable by the normally used LOS tests with a single fault activation cycle. For most of the circuits the percentage of pseudo-functionally detectable faults that are not detected by LOS tests is over 1% and on average 6.5%. This may lead to test escapes that could contribute to field returns.

Table 1: TDFs detected by PFN but not detected by standard LOS

Ckt	# Flts	# Det. PFN - M.	# Det. Std. LOS	# Flts. Esc.	Esc. (%)
s1488	2770	2728	2211	547	20.05
s1494	2810	2753	2225	558	20.27
s5378	7040	5431	6522	262	4.82
s9234	11328	6939	9882	74	1.07
s13207	15602	10801	13377	595	5.51
s15850	19046	13406	17176	352	2.63
s35932	63502	56257	56446	0	0.00
s38417	49738	48577	48560	910	1.87
s38584	61254	55719	56118	1383	2.48
average					6.52

Next we investigated if using multiple fault activation cycles in LOS tests could detect the pseudo-functionally detectable faults. Results of this experiment are given in Table 2. After the circuit name we give the number of TDFs that are detected by pseudo-functional tests using up to 11 fault activation cycles followed by the number of pseudo-functionally detectable faults that are not detected by the LOS tests using multiple fault activation cycles. In the last column we give the percentage of pseudo-functionally detectable faults which are not detected by the LOS tests using multiple fault activation cycles. From Table 2 it can be noted that in most of the circuits all pseudo-functionally detectable TDFs are detected by LOS tests using multiple fault activation cycles.

Table 2: TDFs detected by PFN but not detected by LOS using multiple fault activation cycles

Ckt	# Flts	# Det. PFN - M.	# Det. LOS - M.	# Flts. Esc.	Esc. (%)
s1488	2770	2728	2770	0	0.00
s1494	2810	2753	2794	0	0.00
s5378	7040	5431	6960	0	0.00
s9234	11328	6939	10698	0	0.00
s13207	15602	10801	15333	28	0.26
s15850	19046	13406	18343	34	0.25
s35932	63502	56257	56446	0	0.00
s38417	49738	48577	49544	0	0.00
s38584	61254	55719	58963	8	0.01
average					0.06

To provide a complete analysis of the effects of using LOS tests as part of manufacturing tests for VLSI designs we extract the data on over testing by LOS tests given in [12]. To measure over testing by LOS tests, we determined the numbers of TDFs that are not detectable by pseudo-functional tests but are detected by LOS tests using 1 through 11 fault activation cycles. We give the results of this experiment in Table 3. After the circuit name we give the number of TDFs detected by LOS tests but are not detectable by pseudo-functional tests. The numbers of detected faults by LOS tests using 1 through 11 fault activation cycles are given in different columns with the number of activation cycles shown. It can be seen that for all circuits overwhelming majority of pseudo-functional undetectable faults are detected by the standard LOS tests using single fault activation cycle which is the minimum number of activation cycles needed. Thus over testing by LOS tests does increase negligibly when multiple fault activation cycles are used to eliminate under testing. Thus if one uses LOS tests to detect delay faults due to their advantages in run times, pattern counts and fault coverages then one should also consider using multiple fault activation cycles to eliminate under testing.

Table 3: TDFs not detectable by pseudo-functional tests and detected by LOS tests

Circuit	Total	Number of faults detected 1	2	3	4	5	6	7	8	9	10	11
s1423	38	37	0	0	0	1	0	0	0	0	0	0
s1488	42	30	7	4	0	1	0	0	0	0	0	0
s1494	41	30	7	3	0	1	0	0	0	0	0	0
s5378	1529	1353	131	31	8	5	0	0	1	0	0	0
s9234	3759	3557	149	20	13	7	5	3	2	2	1	0
s13207	4578	3826	308	60	45	38	52	58	56	131	2	2
s15850	4943	4294	298	70	79	80	35	5	76	4	1	1
s35932	189	189	0	0	0	0	0	0	0	0	0	0
s38417	967	904	41	13	2	1	2	2	2	0	0	0
s38584	3250	2768	182	16	27	32	121	86	18	0	0	0

The findings from the results reported in Tables 1 through 3 can be summarized as follows. The normally used LOS tests employing single fault activation cycle fail to detect substantial numbers of TDFs that may cause circuit malfunction in normal operation. However essentially all such faults can be detected using LOS tests with multiple fault activation cycles. Further more the reduction/elimination of under testing is obtained with negligible increase in over testing which is normally attributed to LOS tests.

5. Conclusions

In this work we report, for the first time, the potential for test escapes using standard launch off shift tests to detect delay faults. The test escapes caused by the LOS tests that use single fault activation cycles not detecting delay faults that could cause circuit malfunction during

normal operation. We also showed that the test escapes can be essentially avoided if LOS tests with multiple fault activation cycles are used.

References

[1] J. Savir, "Skew-Load Transition Test: Part I, Calculus", Proc. ITC 1992, pp. 705-713.
[2] J. Savir and S. Patil, "Broad-Side Delay Test", IEEE Trans. on Computer-Aided Design 1994, pp. 1057-1064.
[3] S. Dasgupta, R. G. Walther, T. W. Williams and E. B. Eichelberger, "An Enhancement to LSSD and Some Applications of LSSD in Reliability, Availability and Serviceability", Proc. FTCS 1981, pp. 880-885.
[4] J. Rearick, "Too Much Delay Fault Coverage Is a Bad Thing", Proc. ITC 2001, pp. 624 – 633.
[5] S. Patil and N. Tendolkar, "Delay Testing: Theory and Practice", VTS 2006 Tutorial.
[6] I. Pomeranz and S.M. Reddy, "On application of output masking to undetectable faults in synchronous sequential circuits with Design-For-Testability logic", Proc. ICCAD 2003, pp. 867-872.
[7] I. Pomeranz, "On the Generation of Scan-based Test Sets with Reachable States for Tests under Functional Operation Conditions"' Proc. DAC 2004, pp. 928-933.
[8] I. Pomeranz and S. M. Reddy, "Generation of Functional Broadside Tests for Transition Faults", IEEE TCAD, 2005.
[9] G. Chen, S. M. Reddy and I. Pomeranz, "Procedures for Identifying Untestable and Redundant Transition Faults in Synchronous Sequential Circuits", Proc. ICCD 2003, pp. 36-41.
[10] Y.-C. Lin, F. Lu, K. Yang, and K.-T. Cheng, "Constraint Extraction for Pseudo-Functional Scan-based Delay Testing", in Proc. ASP-DAC, Jan. 2005, pp. 166 – 171.
[11] Z. Zhang, S.M. Reddy and I. Pomeranz, "On Generating Pseudo-functional Delay Fault Tests for Scan Designs," Proc. DFTS 2005, pp. 398-405.
[12] Z. Zhang, S. M. Reddy, I. Pomeranz, X. Lin and J. Rajski, "Scan Tests with Multiple Fault Activation Cycles for Delay Faults", Proc. VTS 2006, pp. 343-348.
[13] J. Abraham, U. Goel and A. Kumar, "Multi-Cycle Sensitizable Transition Delay Faults", Proc. VTS 2006, pp. 306-311.
[14] K.-T. Cheng "Transition Fault Testing for Sequential Circuits", IEEE Trans. on Computer-Aided Design, Dec. 1993, pp. 1971 – 1983.