Low Power Techniques for Mobile Application SoCs Based on Integrated Platform "UniPhier"

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Abstract

In this Paper, we describe the various low power techniques for mobile application SoCs based on the integrated platform "UniPhier". To minimize SoC power dissipation, hierarchical approaches from UniPhier Soc level, UniPhier Processor level, IPP (Instruction Parallel Processor) level, and Circuit level are adopted. As SoC level, 1) Well functionally isolated 5 major units of UniPhier SoC architecture, 2) Dedicated stream DMA controller which can minimize CPU load and memory access. As UniPhier Processor level, 1) UniPhier Processor consists of IPP with dedicated low power hardware engine, 2) VMP (Virtual Multi-Processor) mechanism with micro sleep which can reduce average power consumption in case of multiple tasks concurrent operation, 3) Intermittent operation with the combination of micro-sleep and clock/power down scheme in case of very light load operation. As IPP level, 1) Sophisticated instruction fetch buffer mechanism which can reduce more than 50% memory access for instruction fetch. 2) Hierarchical and selective clock gating scheme by detailed clock power analysis and clock activity rate analysis on real application,) Optimized physical implementation with low-power library and selective use of custom macros. As circuit level, mixed body bias technique with fixed Id and fixed Vt control which can realize 85 % delay variation suppressed and 25% ED product improvement compared with the No body bias.

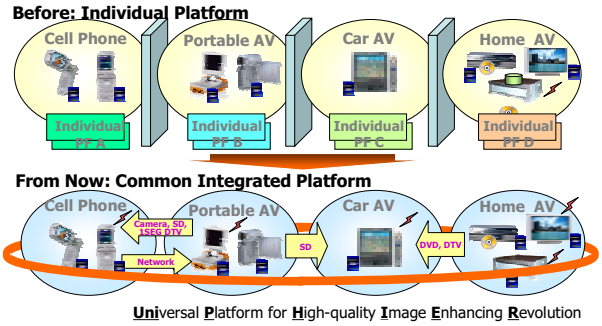

Fig. 1. UniPhier Platform concepts

Introduction

UniPhier is the strategic integrated platform for digital consumer applications and it is introduced into very wide range of consumer products, mobile applications, personal AV applications and Car/Home AV applications, shown in Fig. 1.[1][2]

Purposes of introduction of UniPhier Platform are 1) realizing a breakthrough of technology barrier between individual platforms for each product category, 2) solving the explosion of software development by common architecture over segmented product category, and 3) increasing productivity and design quality.

UniPhier Platform consists of both of hardware and software platform. UniPhier hardware platform is based on scalable media processor, called UniPhier Processor, with IPP (Instruction Parallel Processor) and dedicated hardware engines. UniPhier software platform is for both CPU's application software and IPP's media software.

Low power SoCs based on UniPhier Platform are realized by the combination of a lot of low power

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techniques of various levels, SoC architecture level, UniPhier Processor level, commonly used media processor (called, IPP) level, and dedicated circuit level.

SoC Level Low Power Techniques

Fig. 2 Shows a UniPhier Platform-based SoC architecture and scalable UniPhier processor variations for three major product categories.

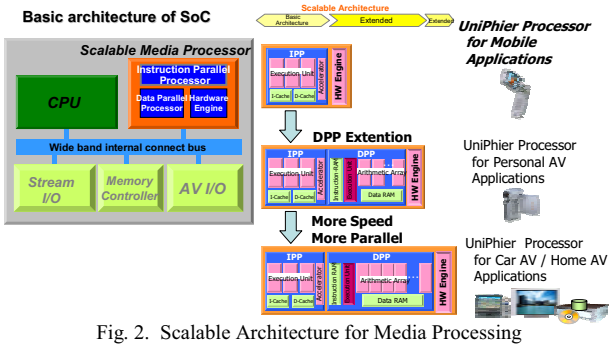


Fig. 2. Scalable Architecture for Media Processing

UniPhier Platform-based SoC consists of five major unit, UniPhier Processor, CPU, Stream I/O, AV I/O and memory controller. These five units are connected by wide range high bandwidth interconnect. UniPhier hardware Platform can provide a suitable configuration of UniPhier processor as a system required AV components and can provide a common architecture for Stream I/O, AV I/O and memory controller to customize for each category requirements.

To reduce power at the SoC level, one of the most important things is to map the system on SoC hardware suitably by understanding the system behavior very well. Well-functionally isolated five major units of UniPhier Platform are very effective for mapping system on SoC hardware. Second one is to reduce the external memory access realized by high band-width internal connect bus with on-chip memory. Third one is to reduce CPU load as much as possible realized by dedicated stream DMA Controller which can treat bit stream operation effectively and can transfer AV stream data from memory to UniPhier Processor directly.

UniPhier Processor Level Low Power Techniques

As shown in Fig.2. UniPhier Processor has some variations for each product category, like IPP with multiple DPPs (Data Parallel Processor) and dedicated hardware engines for car / home AV category, IPP with single DPP and dedicated hardware engines for personal AV category, IPP with simple dedicated engines for mobile category. Even there are some architectural differences on those three UniPhier processors, but software structure is completely same for all of UniPhier processors.[1][2][3]

For mobile category applications, we introduced the simplest UniPhier processor architecture to make block level clock gating control or block level power down control much easier. Dedicated hardware implementation for standard AV codec algorithm is the most effective way to minimize power rather than programmable hardware approach or processor-based approach.

Generally, power dissipation of the dedicated hardware engine is the minimum rather than processor-based approach, but it is very hard to realize full AV system without any processor. On UniPhier processor architecture we adopt combinational approach with IPP plus dedicated hardware engines for mobile application so it is very important to reduce power dissipation of IPP to reduce total power dissipation of AV codec system. Two schemes, one for average power reduction in case of heavy load and multiple task operations like 1-seg DTV and any other applications, another for minimizing power in case of very light load operation, like SD audio, are introduced.

For average power reduction in case of heavy load, we adopt micro-sleep with VMP (Virtual Multi-Processing) mechanism. As features of VMP, a) It supports a coarse grain hardware multi threading, contexts of each thread are stored on on-chip context memory and context switching is automatically done by hardware control, b) It supports a coarse grain hardware thread scheduling, performance assignment for each thread is guaranteed by hardware scheduling and two types of scheduling, time-based scheduling and event driven scheduling are supported. By using VMP mechanism, even heavy and multiple tasks work concurrently, we can guarantee the assigned performance for each thread to realize

real-time system without real-time OS.

As a real-time system design, worst case performance has to be assigned for each thread, but the worst performance is not continuously required. In this case, micro-sleep is very efficient to reduce average power as shown in Fig. 3. Each thread can stop his clock by using VMPWAIT instruction independently from other threads and can be wakened up by external event. By combination of VMP and micro-sleep, we can guarantee both of real time system and minimization of average performance in case of heavy load.

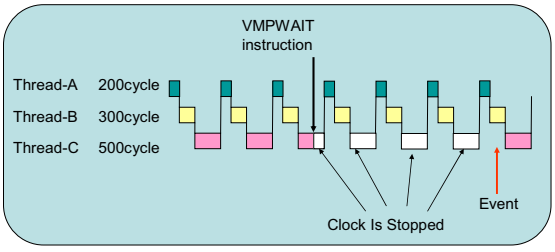


Fig. 3. micro-sleep with VMP (Virtual Multi-Processing)

Current mobile SoC requires not only average power reduction in case of heavy and multiple tasks concurrent operation, but also minimal power consumption in case of very light load operation. For this, intermittent operation with the combination of micro-sleep and voltage down scheme is adopted. IPP is used only for decoding portion of SD audio system and performance requirements is less than 7% of whole IPP performance even assuming worst case and the average performance is less than 4%. So nominal voltage power is supplied only 7% for activating IPP to guarantee decoding operation and other 93% is minimal voltage is supplied to reduce leak power and within activated cycle micro sleep helps to reduce average power, as shown in Fig. 4.

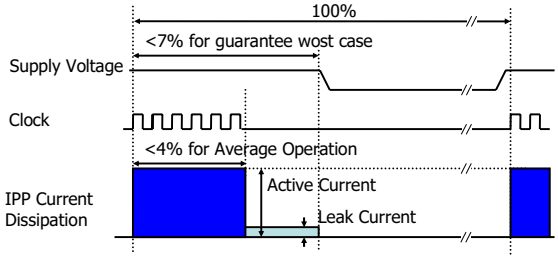


Fig. 4. Intermittent operation with micro-sleep

IPP Level Low Power Techniques

IPP (Instruction Parallel Processor) is a unique media processor[3] and supports three instructions issue. SoCs based on UniPhier Platform always include IPP core on it, because of the multi-media software distribution beyond product categories. So, power reduction of IPP itself is also most important. We explain three schemes to reduce IPP power, one is micro-architectural approach, one is clock gating scheme, and another is implementation approach.

For processor, power dissipation caused by memory access, especially instruction cache or memory access is one of the biggest portions. For example, our proprietary low power embedded CPU core consumes more than 20% of total power consumption.[4] So power reduction caused by instruction access is very important. IPP adopts sophisticated instruction fetch buffer mechanism as shown in Fig. 5.

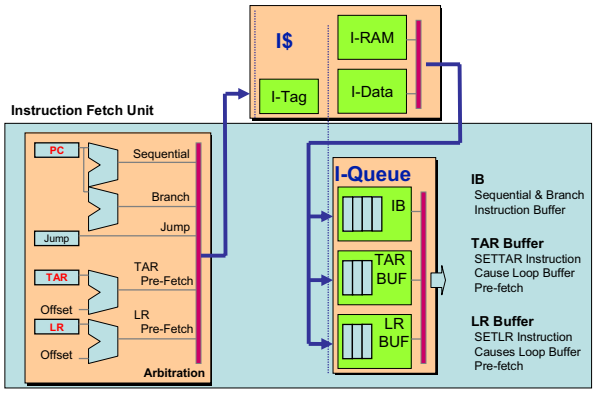


Fig. 5. Organization of Instruction Fetch Unit

Instruction fetch unit has 2 blocks, instruction address generation block and instruction queue block. The instruction address generation block consists of sequential and branch address generator and two types of instruction pre-fetching address generator. The instruction queue block consists of sequential instruction buffer (IB) and two types of loop buffers (TAR buffer / LR Buffer) for pre-fetched instructions. In normal sequence, only IB is used as instruction buffer and TAR and LR buffers are used as hidden loop pre-fetch buffer initiated by dedicated instruction. In loop

operation, instructions are provided from loop buffer and IB works as an extension of loop buffer. If all of instructions can be kept in loop buffer and IB, there is no instruction cache access. We analyzed a lot of media applications to find suitable buffer size. Finally we decided that IB is 16 byte times 4 and loop buffer is 16 byte times 3 as an optimal size and instruction access is reduced to less than 50%.

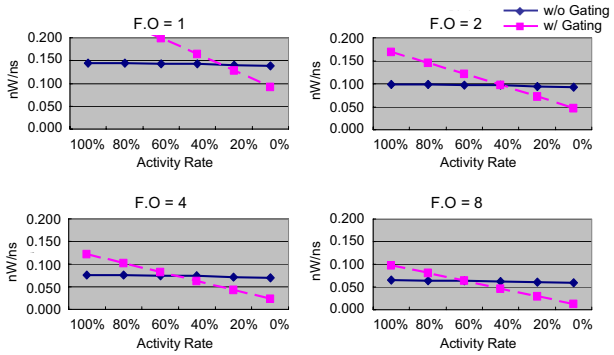


Fig. 6. Power Comparison for fan-out variation of clock gating

Clock gating is very conventional approach to reduce power but it is necessary to put clock gating properly. We analyzed an effectiveness of power reduction with balance of number of fan-out and clock activity rate. This heavily depends on process and circuit implementation of clock gating. Fig. 6 shows an example of power comparison for fan-out variation 1, 2, 4, and 8 of clock gating.

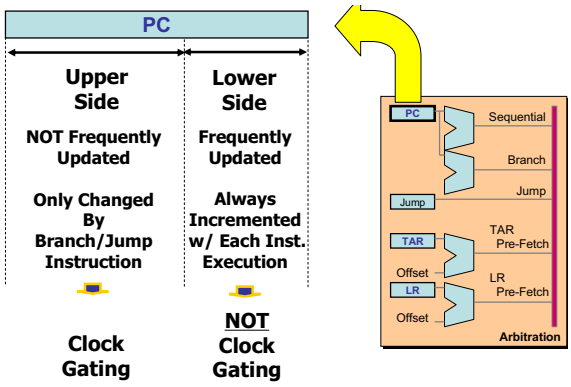
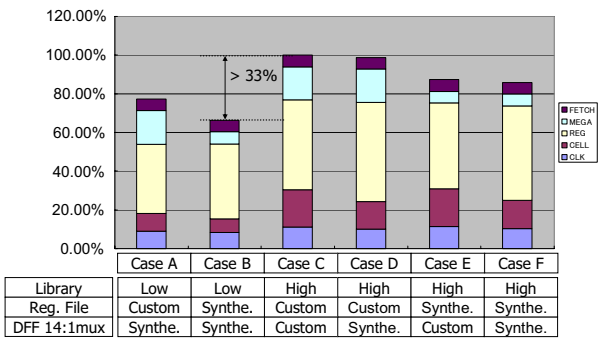


Fig. 7. An example of selective clock gating

In this practice, we found that even if fan-out = 8 activity rate has to be less than 50% to reduce power by clock gating. We also analyzed activity rate of each DFF very carefully at running a lot of media applications. Even average activity rate of each module are varied from 16% to 99%. Based on these analyses we decided to put clock gating selectively for each DFF and finally just 77.9% of DFFs are gated to minimize total clock power. Fig. 7 shows an example of selective clock gating. It shows clock gating for PC (Program Counter) portion.

IPP is commonly used for wide range product category, because of software re-usability. So software compatibility has to be kept but hardware implementation can be optimized for each application. To optimize physical implementation for both performance side and low power side, we prepare two type of logic libraries, high speed library or low-power library and also prepare two of custom modules for high performance, multi-banked register file[5] and Dynamic DFF with 14:1 mux[6]. We can selectively use any components for each application. Fig. 8 shows the power comparison results for each configuration.



	Case A	Case B	Case C	Case D	Case E	Case F
Library	Low	Low	High	High	High	High
Reg. File	Custom	Synthe.	Custom	Custom	Synthe.	Synthe.
DFF 14:1mux	Synthe.	Synthe.	Custom	Synthe.	Custom	Synthe.

Fig. 8. Power comparison for each configuration

Performance difference between case B and case C is only 15%, but by optimizing physical implementation with low-power library and selective use of custom macros, power dissipation can be reduced more than 33%.

Circuit Level Low Power Techniques

As circuit level low power technique, we introduce mixed body bias technique with fixed Id and fixed Vt control[7]. Fig. 9 shows a test chip to which the proposed mixed body bias control techniques are applied.

This test chip consists of a CPU control logic block, a register file, a data path, and an SRAM block.

Each block has a circuit structure defined by its functional requirements and uses devices with Vt set according to the activity of the block. For example, the register file and data path use domino circuits, and the SRAM uses high Vt devices. The optimum body biases for each circuit are generated by the fixed Vt and fixed Ids body bias generator. In addition, these body bias generators are independent for each Vt devices.

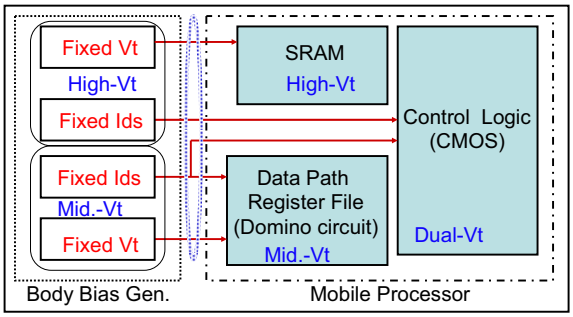


Fig. 9. Mixed body bias techniques

By measuring this test chip, results of the register file for each body bias scheme is shown as Fig. 10. By adopting proposed mixed body bias technique, we can show that 85 % delay variation suppressed and 25% ED product improvement compared with the NO body bias.

Register File	Power	Yield		Test Cost
	ED Product (vs. NBB)	Delay Variation (vs. NBB)	Noise Margin	Delay Temp. Depend
No Body Bias	1.00	1.00	Low	Flat or Negative
Only Fixed Vt	0.92	0.48	High	Positive
Only Fixed Ids	0.80	0.12	Low	Flat or Negative
★ Mixed Body Bias	0.75	0.15	High	Positive

Fig. 10. Effect of each body bias scheme (Relative Ratio)

Conclusion

In case of development of UniPhier-based SoC for mobile application, we can pick the combination of suitable low power techniques to realize the target and we can provide a good trade-off between power and area and cost.

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