Simple and Accurate Models for Capacitance Increment due to Metal Fill Insertion

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Abstract – Inserting metal fill to improve inter-level dielectric thickness planarity is an essential part of the modern design process. However, the inserted fill shapes impact the performance of signal interconnect by increasing capacitance. In this paper, we analyze and model the impact of the metal dummy on the signal capacitance with various parameters including their electrical characteristic, signal dimensions, and dummy shape and dimensions. Fill has differing impact on interconnects depending on whether the signal of interest is in the same layer as the fill or not. In particular intra-layer dummy has its greatest impact on coupling capacitance while inter-layer dummy has more impact on the ground capacitance component. Based on an analysis of fill impact on capacitance, we propose simple capacitance increment models (Cc for intra-layer dummy and Cg for inter-layer dummy). To consider the realistic case with both signals and metal fill in adjacent layers, we apply a weighting function approach in the ground capacitance model. We verify this model using simple test patterns and benchmark circuits and find that the models match well with field solver results (1.2% average error with much faster runtime than commercial extraction tools, the runtime overhead reduced by ~75% for all benchmark circuits).

I. Introduction

Chemical mechanical polishing, when combined with dummy metal fill, has become an essential process step to minimize interlevel dielectric (ILD) thickness variations in modern VLSI designs [1]. Increasing numbers of metallization levels exacerbates the requirements for both CMP and metal fill insertion approaches [2]. Metal fill insertion has been widely adopted to increase planarity but creates new problems in timing and silicon verification [3]. The impact on interconnect capacitance leads to a significant influence on delay, coupling, crosstalk noise, and power consumption. Fill patterns rely on either grounded or floating metal and there are unique modeling difficulties with either of these techniques [5]. Accuracy of parasitic extraction of full-chip without dummy patterns has become critical because dummy is typically inserted at the tape-out stage. Ad hoc insertion of metal fill without proper consideration of the impact on signal line capacitance may lead to performance degradation or outright chip failure. Therefore, the understanding of the impact of dummy fill, the extraction of the correct parasitics given fill, and the availability of optimization techniques to achieve minimum performance degradation while promising the required planarity are desired.

II. Prior Work

Stine et al. [5] proposed rule-based filling methods and provided general insertion guidelines based on the analysis of the impact of metal fill on interconnect capacitance. Key issues in dictating metal fill are buffer distance, grounded versus floating, and the shape of fill patterns. A more complete analysis considering many possible parameters such as on- and off-plane, buffer space, filler size, and signal width/space is available in [6],[7]. They point out that buffer space, filler density, signal dimensions, and ILD thickness are major factors in interconnect capacitance increase by dummy fills. Results indicate that smaller buffer space, larger filler size, wide and bigger signal line space result in larger increase of interconnect capacitance by dummy. And off-plane dummy-fills have bigger impact than on-plane dummy. They claim that 3~4% increase in delay with dummy in average and 25% increase in maximum for full chip simulations.

[19] analyzes the impact on total capacitance and coupling capacitance between signal lines by dummy. They also measure the influence on the signal delay and crosstalk noise by dummy. Authors claim that propagation delay can be increased more than 20% by dummy. And crosstalk noise analysis provides the importance of inter-layer dummy than intra-layer dummy because current designs have sufficient buffer space between signal lines and dummy.

Generic capacitance models have been proposed to account for the impact of grounded or floating dummy [5]. Each capacitance component, such as coupling between active lines and dummy metals or ground capacitance, can be approximated using simple closed-form expressions.

[6],[7] propose a technology modification method to include the dummy fill impact at the full-chip extraction stage. An equivalent ILD permittivity value can be obtained by fitting the simulation results of structures having off-plane dummy using a 3D field solver. These higher permittivities (e.g., 23~30) replace the original dielectrics as conformal layers. The permittivity values depend on the density of dummy-fills and height of the metal layers. Then a full-chip extraction tool targeting this modified technology can be employed to measure accurate parasitics of original layouts preceding dummy fill.

In [19] the authors propose a new capacitance model based on the idea of reducing the thickness of dummy metals. They calculate the capacitance of signal lines by ignoring the thickness of metal fill because the capacitance of parallel planes with a floating conductor between them is equal to their capacitance excluding the thickness of the conductors. A comparison between silicon measurement data and models shows < 8% errors.

The remainder of this paper is organized as follows. Section III analyzes the impact of metal fill insertion on interconnect capacitance and Section IV describes the construction of capacitance increment models based on observations in Section III. We present detailed simulation results to verify these models in Section V, and Section VI concludes the paper.

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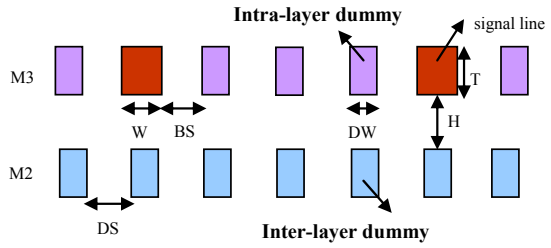


Figure 1. Cross-sectional view of two layers of interconnect with metal fills.

III. Analysis of Metal Fill and Guidelines

We use *QuickCap* [21] as a Golden tool to extract and analyze the capacitance impact due to dummy fill, both for floating and grounded fill. The 'float' command is used for floating dummy extraction. The accuracy parameter is set '1%' to provide a balance between accuracy and runtime.

The cross-sectional view of a two layer (M2, M3) interconnect structure is shown in Figure 1. Here W is the width of the signal lines of interest, BS is the buffer distance (i.e., the minimum distance from the signal line to the metal dummy), DW is the dummy width, DS is the space between dummies, H is dielectric height, and T is metal thickness.

All interconnect parameters are based on the International Technology Roadmap for Semiconductors at the 130nm technology node [20]. Structures with 3 metal layers (M2, M3, and M4) and 3 signal lines in M3 are generated and dummy patterns of different shapes are inserted into the layouts manually. All parameters are included in Table I.

There are numerous dummy parameters that impact interconnect capacitance. In addition to whether the fill is grounded or floating, we consider other key parameters including buffer space, fill density, signal line dimensions (signal line width and space), metal dummy dimensions (dummy width and space), and the shape of the dummy pattern.

A. Electrical property (Grounded vs. floating)

Figure 2 shows the total capacitance increment for the two dummy types (grounded and floating) at two different signal widths. As is expected, grounded metal fills have a much higher influence on capacitance than floating dummies. Wider signal lines (e.g., W=2um) is more susceptible to the grounded metal fills but there is not much dependency on the signal width in the floating case. In both cases, the impact increases as the signal line spacing increases. The floating dummy metals show ~12% impact on the interconnect capacitance in this example.

Though grounded metal-fills are more stable and easy to extract they are not desirable due to both their higher impact on capacitance and also routing difficulties in current technology nodes [5]. Therefore we focus on floating dummy fill when building models for interconnect capacitance and generate these models either for intra-layer and inter-layer scenarios.

TABLE I
Interconnect and metal-fills parameters for the analysis

Parameters	Values
Signal Width(W)	0.2, 0.5, 1, 2um
Signal Space(S)	0.2, 0.5, 1, 2, 3, 4, 5um
Metal Thickness(T)	0.31um
Dielectric Height(H)	0.32um
Buffer Space(BS)	0.4, 0.6, 0.8, 1.0um
Square Dummy Width(DW)	0.2, 0.6, 1.0, 1.5um
Square Dummy Space(DS)	0.1, 0.3, 0.5, 0.7um
Dummy-fill density(ρ)	20, 40, 60, 80, 100%
IMD(inter-metal dielectric)	2.9
ILD(inter-layer dielectric)	3.27

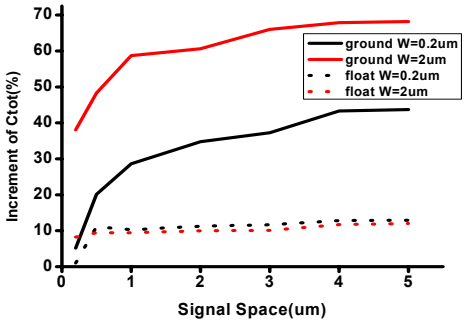


Figure 2. Impact of ground vs. floating metal dummy on the interconnects (DW=0.6um, BS=0.6um, density=60%)

B. Intra-layer vs. inter-layer

(a) in Figure 3 shows the impact of each capacitance component due to intra-layer dummy fill (i.e., dummy at the same layer as signals of interest). As can be seen from the graph, there is negligible impact on the ground capacitance component due to intra-layer dummy but the coupling capacitance is strongly affected. However, the relative portion in total capacitance is small for the coupling capacitance when signal space is large. Buffer space and dummy density (dummy space and dummy width) are important factors.

(b) in Figure 3 shows the impact on each capacitance component due to the presence of inter-layer dummy fill (i.e., dummy patterns on adjacent layers). Here inter-layer dummy has impact on both coupling and ground capacitance components. Again though, as the Cc component in Ctot gets smaller as the space increases (less than 1/10 of Cg), the total capacitance increment is mainly due to the impact on the ground capacitance component with inter-layer floating dummies.

C. Buffer space

Buffer space is defined as the minimum distance allowed between signal lines and metal fill. The increase in total capacitance for different buffer spacings in the intra-layer floating dummy case is shown at (c) in Figure 3. The figure shows that buffer space is the one of the major factors in

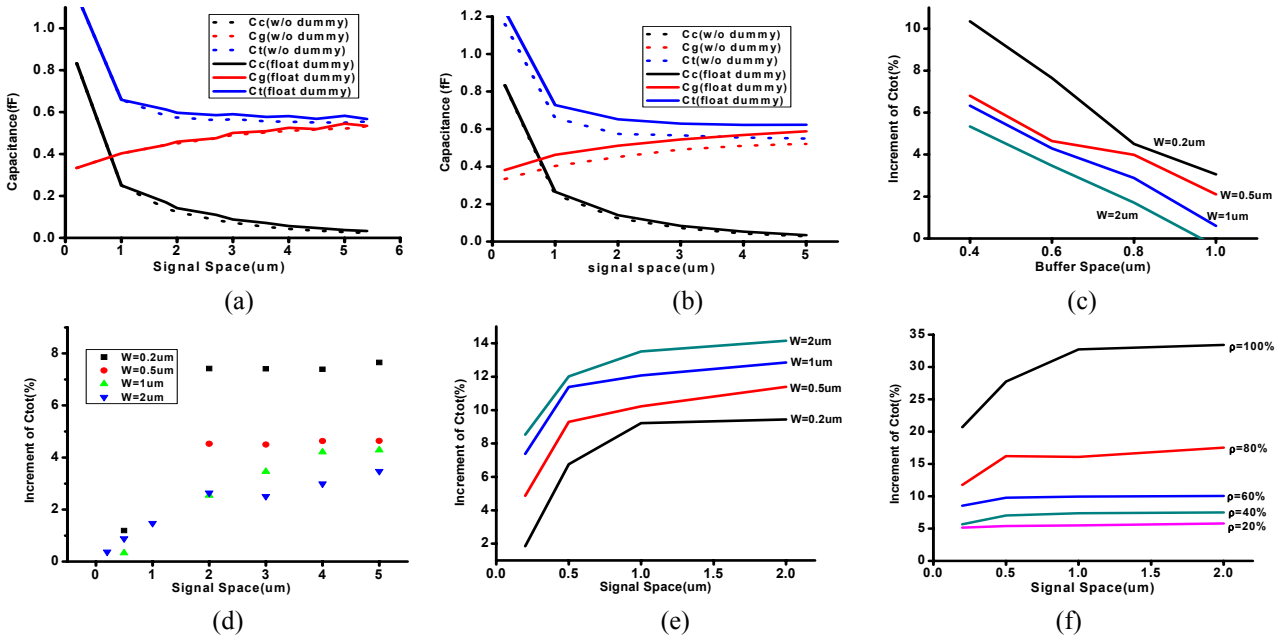


Figure 3. Impact on the interconnect capacitance by floating metal dummy in different parameters; (a) intra-layer floating metal dummy, (b) inter-layer floating dummy, (c) buffer space for different signal width, (d) signal width and space by intra-layer floating dummy, (e) signal width and space by inter-layer floating dummy, (f) metal-fills density at inter-layer.

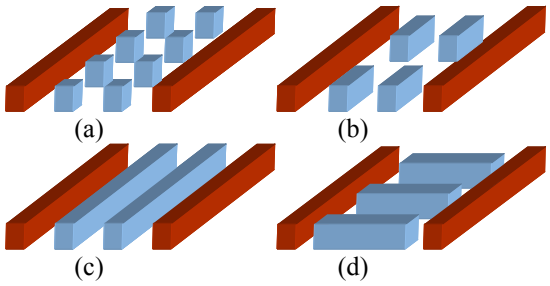


Figure 4. Possible dummy shapes; (a) square, (b) rectangular, (c) parallel line, and (d) orthogonal dummy.

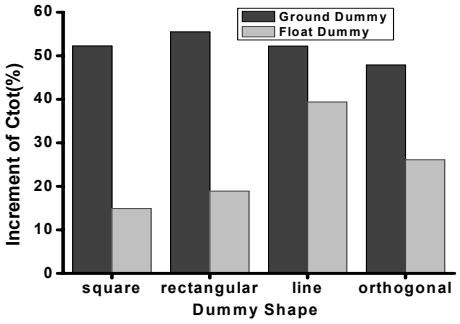


Figure 5. Total capacitance increments with different metal dummy shapes

determining capacitance. As expected, impact reduces as the buffer space increases. The increment of Ctot can be reduced by more than 50% when buffer space rises from 0.4um to 0.8um.

D. Signal width and space

(d) and (e) in Figure 3 examine the role of signal width and space on the capacitance increment due to floating dummy (both intra-layer and inter-layer). In both cases the total capacitance increases as the signal space increase. However intra-layer dummy saturates around the point when the spacing becomes sufficient to insert dummy patterns between signal lines. For inter-layer dummy, the total capacitance increment does not change appreciably when the space is >1um. It is interesting that for the intra-layer dummy the total capacitance increment reduces for larger signal widths. This is mainly because in wide lines the greatest portion of capacitance is to ground and the coupling capacitance component is being impacted by fill in this case.

E. Dummy fill density

(f) in Figure 3 shows the total capacitance increment for floating dummy at different densities (ρ) calculated one layer below the signal. A 100% dummy density means all the space is occupied by the dummy metals in a certain window which is usually 100um by 100um or 200um by 200um area. Here 20% fill density implies that there are 80% signals lines and rest of the area is for dummy metals. As can be seen from the graph, there is a strong dependency of interconnect capacitance on dummy density. The impact of floating metal-fills decreases <10% where the metal dummy occupy less than 60% of the specific window size.

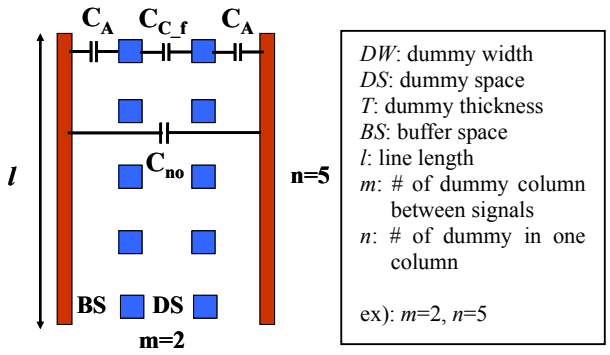


Figure 6. Parallel plate model for coupling capacitance increment model by intra-layer metal-fills, (note that there are two interconnect lines and two columns of square metal fills with each column having 5 metal pieces)

F. Dummy shape and dimension.

Figure 5 presents the total capacitance increments for different dummy shapes which are shown in Figure 4 in grounded and floating metal-fill types. For grounded dummy, although the rectangular shape shows the worst impact, the dummy shape does not affect the capacitance variation. On the other hand, for floating dummy there are higher variations between dummy shapes. The parallel line dummy structure results in the worst impact on signal capacitance (~40%) whereas square dummy patterns provide the smallest impact (~15%). Therefore, to reduce the number of dummy patterns, rectangular or orthogonal shape of dummy structures is preferred over parallel lines.

IV. Capacitance Increment Models

A. Intra-layer dummy

First, as mentioned in the previous section for analysis, there is negligible impact on signals when buffer space is larger than 1um and the impact is greater on Cc than Cg. Therefore, we focus on a model for the coupling capacitance change. For the coupling capacitance, the parallel plate capacitance model can be applied [4]. As described in Figure 6, the coupling capacitance increment model can be formulated as

$$\begin{aligned} C_c(\text{w/ dummy}) &= C_c(\text{w/o dummy}) + C_{c\_inc}(\text{intra}) \\ &= C_{no} \times (l - DW \times n) + C_{dummy} \times DW \times n \end{aligned}$$

$$C_{dummy}(F/um) = \frac{\varepsilon \cdot T}{2BS + DS} \quad ;\text{when m=2} \qquad (1)$$

$$C_{dummy}(F/um) = \frac{\varepsilon \cdot T}{2BS + (m-1)DS}$$

$$\therefore C_{c\_inc}(F) = \frac{\varepsilon \cdot T}{2BS + (m-1)DS} \times DW \times n \qquad (2)$$

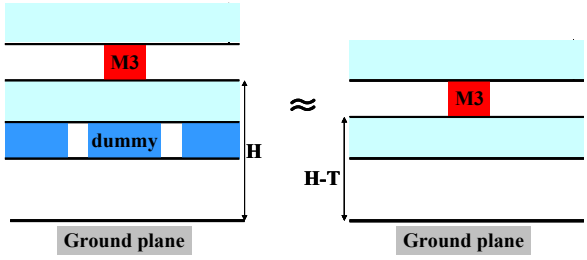


Figure 7. Approximation of the ground capacitance increment model by excluding the thickness of the metal-fill layer.

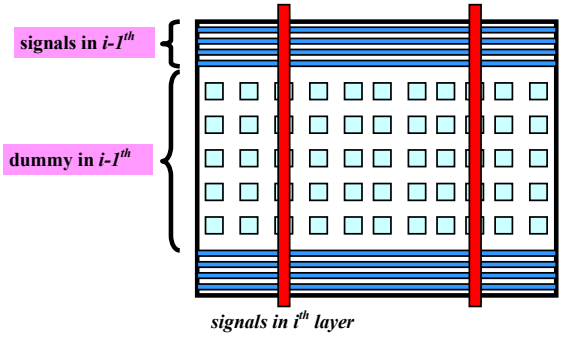


Figure 8. Ratio of dummy area to signal space (α) in the i-1th layer within a certain window size

B. Inter-layer dummy

A second observation from Section III is that there is significant impact on Cg due to inter-layer dummy fill. Thus we only model the ground capacitance change due to dummy patterns on other layers. The capacitance of the parallel plate having floating metal in between can be approximated to the capacitance ignoring the thickness of the conductor [19]. Figure 7 shows the cross-sectional structure of the typical interconnect layers with metal dummy. In this figure, M3 is the signal line and there are dummy patterns in M2. The ground capacitance increment model due to inter-layer dummy can be written as;

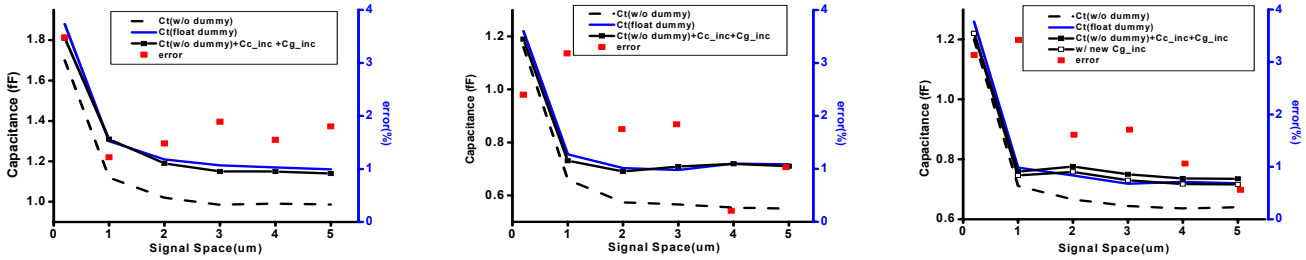
$$\boldsymbol{C_{g\_inc}(\text{inter}) = C_g(H-T) - C_g(H)} \qquad (3)$$

Finally, we can combine the intra-layer and inter-layer dummy models to represent the total capacitance increment model by metal fills considering 3D effects.

$$\begin{aligned} C_{tot}(\text{w/ dummy}) &= C_{tot}(\text{w/o dummy}) + \\ &\quad C_{c\_inc}(\text{intra}) + C_{g\_inc}(\text{inter}) \end{aligned} \qquad (4)$$

$$\left\{ \begin{array}{l} C_{c\_inc}(\text{i}) = \dfrac{\varepsilon \cdot T_i}{2BS_i + (m_i - 1)DS_i} \times DW_i \times n_i \\ C_{g\_inc}(\text{i}) = C_g(H_i - T_{i-1}) - C_g(H_i) \end{array} \right\}$$

However in a real design not all the space under a signal layer is occupied by dummy metals, and it is likely that there



(a) (b) (c)

Figure 9. Total capacitance comparison with proposed models for test cases (a)~(c)

TABLE II
Verification of accuracy and run time of proposed models with the commercial tool in real circuits

Circuits	# of gates	Total nets	Average Ctot (fF)			Errors (%)			Run Time (s)			
			w/o dummy	w/ dummy +FNC	w/ dummy +models	mean	median	95th percentile	w/o dummy	w/ dummy +FNC	w/ dummy +models	savings (%)
c17	11	42	0.52	0.55	0.56	1.1	0.7	2.4	80	165	104	71.8
c432	140	770	1.11	1.30	1.34	1.2	0.6	4.5	120	180	135	75.0
c3540	521	2966	0.83	0.96	0.99	1.1	0.6	3.7	154	248	178	74.5
c6288	2118	13039	1.22	1.47	1.51	1.2	0.7	2.7	583	1177	707	79.1
S	14538	53401	0.48	0.62	0.63	1.3	0.9	4.1	1282	2832	1714	72.1
R	31930	114803	0.53	1.07	1.11	1.0	0.7	2.9	3765	6601	4533	72.9

are orthogonal signal interconnects in the adjacent layers. Figure 8 shows a simple case of two metal layers. There are two vertical signal lines in the i^{th} layer along with other signal lines running horizontally at $i\text{-}1^{th}$ layer. We can define α as the ratio of the metal dummy area to signal space. Then, the above model (4) is still applicable by applying a weighting function (α) to the thickness of the dummy layer. The final ground capacitance increment model for inter-layer dummy can be rewritten as;

$$C_{g\_inc}(\mathbf{i}) = C_g(H_i - \alpha_{i-1}T_{i-1}) - C_g(H_i) \quad (5)$$

Here H is the height from bottom to ground plane and T is thickness of the metal layer and α is the ratio of dummy area to signals in the underlying layer within certain window size.

V. Models Verification

The previous section built models for the incremental capacitance introduced by metal fill, both intra- and inter-layer. To verify the accuracy of these models, we tested them in several simple interconnect structures;

(a) Case1: W=2.0um, DW=0.6um, DS=0.3um, square
(b) Case2: W=0.2um, DW=0.6um, DS=0.3um, orthogonal
(c) Case3: W=0.2um, DW=0.6um, DS=0.3um, α=75%

Figure 9 (a-c) show the total capacitance comparison between field solver results and the proposed capacitance increment models for each test case. The values calculated from the proposed models are shown and the error between the model and simulated results are shown (as data points). As can be seen in all cases, the proposed models show accuracy within 3% throughout the entire signal space range for the chosen test structures. The case (b) in Figure 9 also show that the models are not only valid on square type of dummy but also on rectangular or orthogonal dummy shapes. (c) reveals that applying the simple weighing function (α) in the Cg increment model is an efficiency way of treating the ratio of the inter-layer dummy to the signals.

For circuit-level verification, we generate several layouts using IBM130nm standard cells in a standard auto place & route flow [23]. We then insert 0.6um square floating dummy patterns with 0.3um buffer space in all metal layers to meet density requirements (e.g., 50%). We then use Calibre xRC [22] to extract capacitance both with and without dummy fill considered. This tool includes a parameter "Floating_Net_Coupling" (FNC) to enable the accurate extraction of capacitance in the presence of metal fill. It approximates the effect of the floating nets and computes the effective capacitance to ground at the expense of efficiency. We employ the FNC option to provide a reference for our proposed models. The proposed models are included in the capacitance calculation equations in the technology rule file.

Table II[1] represents the average Ctot values for each circuit and shows the impact of dummy fill for Calibre xRC + FNC and proposed models. The mean, median, and 95th

[1] All runtimes are CPU seconds on a Linux platform of 2 AMD *Opteron* 2.8 GHz with 4GB of RAM per processor.

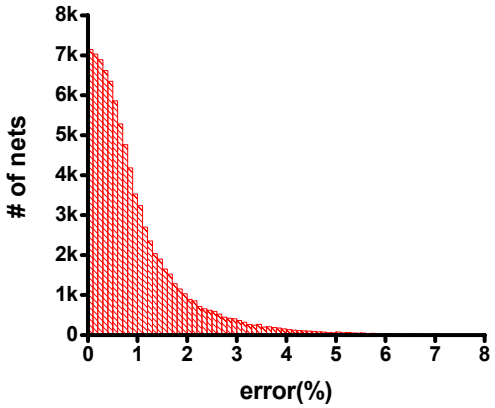


Figure 10. Error histogram over all nets of the circuit R in Table II.

percentile value of error which is computed on a net by net basis are also shown. The error histogram over all nets of the R circuit is provided in Figure 10 to verify that most of the nets have small error with proposed increment models. In all circuits the average error is less than 1.2%. The runtime comparison reveals that the impact of metal fill can be very efficiently considered simply by modifying rule files with the proposed models.

VI. Conclusion

We investigate possible metal dummy parameters in order to develop guidelines that can simplify the development of compact analytical models for capacitance increments. We then propose simple capacitance increment models both for inter-layer and intra-layer dummy fills. If the vertical profile is known after layout, both Cc increment and Cg increment can be modeled using the proposed simple equations. Capacitance increment models are a function of density and design rules (e.g., buffer space, dummy space, and dummy width), as well as metal thickness and dummy occupied space in neighboring layers. Results indicate that the models provide very fast and accurate capacitance calculations compared to current methods built into parasitic extractors. The proposed models can also be applied to guide smart insertion algorithms since they provide fast and accurate prediction of the metal-fill impact.

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