Challenges to Accuracy for the Design of Deep-Submicron RF-CMOS Circuits

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Abstract - Two challenges for the accurate prediction of GHz CMOS analog/RF building blocks are presented. Challenging the usage of new compact MOSFET models enhances the simulation accuracy. The capability of EKV3.0 model has been studied by applying to TOSHIBA's 130nm RF-CMOS technology. The verification facts have shown that EKV3.0 model offered excellent modeling capability of both DC and RF (small and large signal).

Challenging the efficient use of Electro-Magnetic (EM) with one practical setup offered successful prediction of the EM effects in the chip. Enhanced study of EM co-simulation technique that links two challenges had shown the perfect prediction of the TOSHIBA's RF-CMOS circuit (VCO).

I Introduction

The incorporation of as many high-frequency effects (ex. mutual coupling and skin-effect) is a direct key to successful circuit design of RF-CMOS circuits.

Introduction of the "brand-new" compact MOSFET models and efficient use of Electro – Magnetic (EM) simulation offer good opportunity to solve this problem.

By viewing the recent activities done by Compact Model Council (CMC) [1], it can be recognized that compact models should cover accurate prediction of conductance (gm, gds), non-quasi-static (NQS) effect in the weak-inversion region and the incorporation of more numbers of small size effects.

In this paper, adaptation example of EKV3.0 MOSFET model [2,3] to Toshiba's 130nm RF-CMOS technology has presented. Investigations of EKV3.0 model's accuracy has done by the consistent measurement data (containing DC, CV, S-parameter and 2.45 GHz Load-Pull).

Secondly, EM simulation's applicability has studied. EM simulation has rarely used by silicon RF-IC design for a ling time. This is because of the handling difficulty by the EM simulator with the silicon substrate, which has both semi-conductive and semi-insulating nature.

Simple but practical tips described in this paper offers successful prediction of the operation of 2.0GHz voltage-controlled oscillator (VCO).

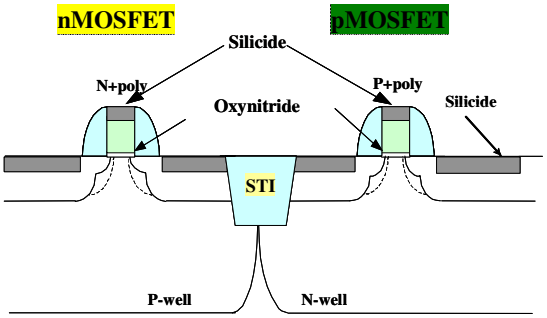

Fig. 1. Cross-sectional view of 0.13um CMOS technology

II. 1st challenge : Introduction of "brand-new" compact MOSFET models.

A. *Accuracy of output conductance of MOSFETs operated in the weak-inversion region.*

Due to the reduction of the power supply voltage, The MOSFETs in the recent analog/RF building blocks are more frequently operated in the weak-inversion region. Eventually, modeling the accuracy in this bias region is very important. We now focus on the normalized output conductance Gs [2,3], which is the essential figure of merit of the MOSFETs' analog behavior.

The definition of Gs [2,3] is shown in the formulae (1), where I_{spec} is the normalized drain current defined by (2), I_D is the drain current, U_T is the thermal voltage (= kT/q), q is the electron charge, ε_{si} is the electron permittivity and N_{sub} is the doping concentration in the silicon substrate.

By taking a close look at (1), it is recognized that Gs depends only on the normalized drain current ($=I_D/ I_{spec}$), meaning that this is a universal description of the MOSFETs' transfer function.

$$G_S = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{I_D}{I_{spec}}}} \qquad (1)$$

$$I_{spec} = 2 \cdot n \cdot U_T^2 \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \qquad (2)$$

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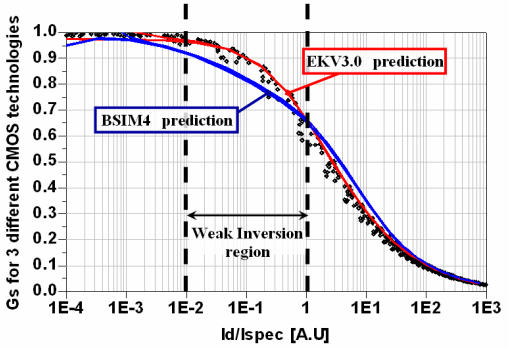

Fig. 2. Comparison of Gs function's prediction by EKV3.0 and BSIM4 compact models. Dots, measured data of 3 technologies nodes (600 nm, 140 nm and 130 nm)

In fig.2, the prediction of Gs between two compact models BSIM4 and EKV3.0 with the measured data of 3 technology nodes is shown. It is possible to recognize that the measurement data belonging to different technology nodes are on the same trace line, indicating that the (1) and (2) is a "born-nature-description" of CMOS devices.

EKV3.0 compact model is currently developed by Technical University of Crete, which denotes the MOSFET behavior by the charge-based approach.

Compact models need to predict correctly this nature. EKV3.0 model fits very well with the measurement in overall region, but BSIM4 models does not offer reasonable prediction specially in the weak inversion region (where ~0.03 < I_d/I_{spec} < ~10) where the most particular correctness is needed for analog-RF design. The standardization procedure is now ongoing process by Compact Model Council [1]. PSP (developed by NXP [4]) and HiSIM (developed by STARC and Hiroshima Univ [5].) have solved this inaccuracy problem as well. It is the designers' choice which compact model is used in the future analog-RF blocks' design.

B. Accuracy of high-frequency-effects of MOSFETs.

Fig.3 illustrates the compact models of MOSFETS for RF extension. Accurate compact model, described in the previous section is placed at the heart adding extrinsic passive elements describing the high-frequency loss. In practical implementations, each value is described by the function of geometrical parameters (such as the gate length, finger length and finger numbers).

Nevertheless, this may not be able to provide sufficient accuracy for the future applications unless compact models correctly handle with the non-quasi-static (NQS) effects. NQS denote the delay of the charge transfer function in the channel [6,7,8], which affects high-frequency behavior of long-channel devices.

Fig.4 shows the comparison of Y21 behavior of long-channel NMOSFET between models and measurement. The NQS function of EKV3.0 model uses channel segmentation approach, offering better prediction of Y21 over 20 GHz frequency range.

Linking the correct implementation of the extrinsic components with accurate compact model, which correctly models NQS effect, it is possible to complete a 1st challenge

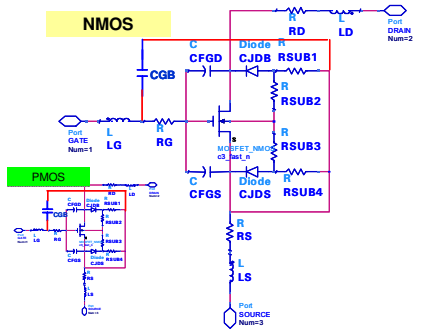

Fig. 3. Implementation example of EKV3.0 macro model for RF extension [9] (source grounded).

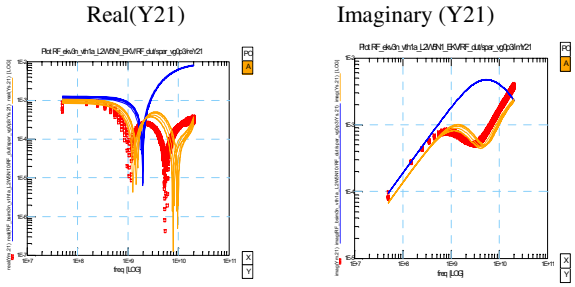

Fig. 4. Comparison of Y21 of BSIM4 (Blue) and (EKV3.0) compact models with the measurement data (red). NMOSFET (130nm RF-CMOS Technology). Vg = 0.3Volts, Vds=0.2,0.3,0.5,0.8,1.1 and 1.4Volts.

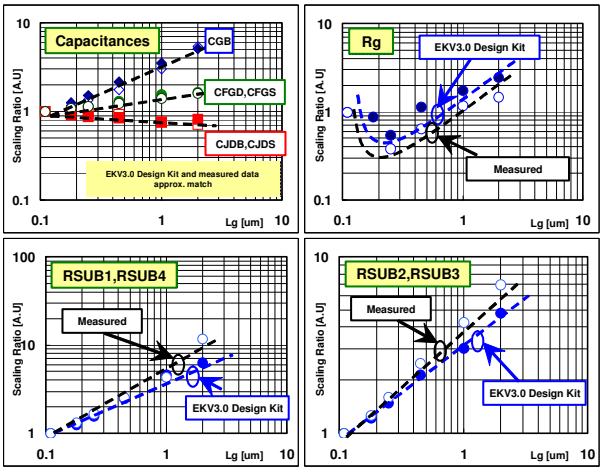

Fig. 5 EKV3.0's prediction of RF scalability showing the estimated gate resistance, substrate resistances, overlap capacitances, and junction capacitances with different gate length (from 0.11um to 2.0um).[9]

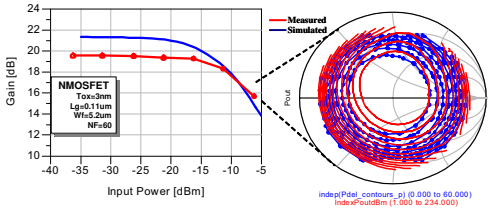

Fig. 6 2.45GHz Load-pull fitting results of EKV3.0 model Lg=0.11um Wf=5.2um, Nf=12, VDS=1.0V, VGS=0.9V. Gain compression and gain contour plot (Gain range 3 dB to 8.5 dB by 0.5 dB)[9,13]

III. 2nd challenge : Efficient use of Electro-Magnetic simulation tool

A. *Preparation of the "substrate file" by using one tip for a better fit with the measurement.*

Recent EM tool offers two types of solutions (full 3 dimensional and 2.5 dimensional). The 2.5 dimensional EM tool is useful for RF-CMOS analog/RF block design. This helps to design input/output matching of the LNA, characterize the on-chip passive components (inductors, capacitors and transformers) and optimize the layout of the voltage-controlled-oscillator (VCO).

EM tools requires input file (substrate file) that provides tool with the cross sectional information of the analyze target. EM-related effects are then calculated based on this information. The creation and calibration of this input file is the most critical and important step in the EM simulation flow.

Quite often, "substrate file" needs modification in pursuit of the perfect accuracy. However, its modification by relying on the simple optimization leads non-realistic and non-physical solutions, which is not accepted by process engineers. Here, 2nd challenge exits. It is the creation of accurate substrate file with the process and fabrication consistency. We will explain the details by the use of Agilent's Momentum [10].

The hollow inductor with 2 turns, shown in the fig.6 is fabricated in 130nm RF-CMOS technology. The configuration is (1) outer/inner length is 166um/120um, (2) track width is 10um, (3) spacing is 3um with (4) 5 stack metal layers.

Cross sectional information used for the Momentum analysis is displayed in the fig.7. Thin conductive layer with the thickness "d" having the same conductivity as the silicon substrate is placed on top of the silicon dielectric layer. These two layers (conductive layer and dielectric layer) configure the silicon substrate. This is a tip for the Momentum use.

Finding an optimum "d" value is necessary to characterize the target process keep the following relationship.

Total thickness of silicon substrate
= d(=thickness of the silicon conductive layer)
+(thickness of the silicon dielectric layer)

The optimum "d" value of 10um was found. Momentum simulation result shown in the fig.8 by using this cross sectional information provided a RMS error below 2.5% for the real part and 2.2% for the imaginary part of S11. Through this investigation, it can be said that EM simulation be applicable to the silicon IC with the adaptation of particular substrate setup.

Testing result of this approach by the use of other process has proved as good accuracy as this case [11]. This means that it is applicable to other processes as well.

B. *Accurate prediction of circuit behavior by the collaboration of two challenges (accurate compact model and EM simulation).*

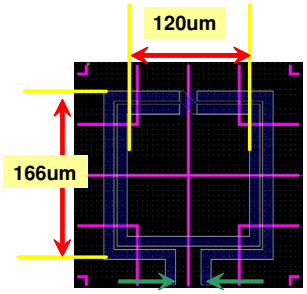

Fig. 6. Layout of on-chip inductor (2 turns) fabricated with 5 metal stack layers fabricated in 130nm RF-CMOS technology.

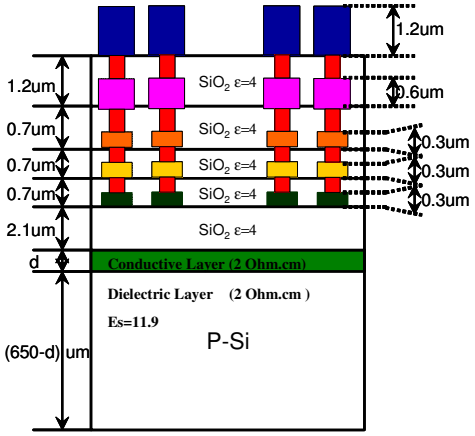

Fig. 7. Cross sectional information of the inductor in the fig.6 used as the setup of Momentum.

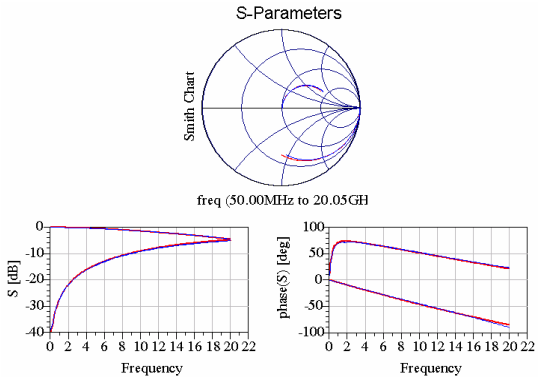

Fig. 8. Comparison of resultant s-parameters between measured (red) and Momentum simulation (blue). Frequency Range : 50MHz ~ 20.05GHz

The adaptation example of two challenges is shown by taking the case of 2GHz CMOS voltage controlled oscillator (VCO) design. The most difficult issue is the layout optimization of the tank circuit which strongly influences the overall characteristics.

Its schematic is displayed in fig. 9. Dotted area represents the main oscillator block. There are CMOS transistors (EKV3.0 model) with different numbers of fingers (unit size:8um/0.4um), one inductor (0.8nH), Metal-Insulator-Metal (MIM) capacitors (20pF) and variable capacitor (32 pF). The configuration of inductor is 2.75 turns and 40um/4um pitch, estimated self inductance by the Greenhouse formula [12] is 0.8 nH. The distance from the guard-ring is 20um.

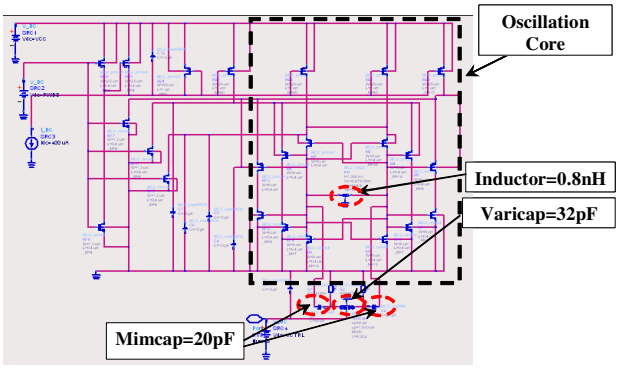

Fig. 9. Circuit schematic of 2GHz RF-CMOS VCO.

The frequency tuning characteristics has been measured by changing the control voltage from 0 v to 2.5 volts by 0.5 volts step. Resultant data is compared with following the simulation.

(Case1) The 7 tones harmonic balance simulation (fig.9)

(Case2) Agilent's EM-Co-Simulation [10] (fig.10)

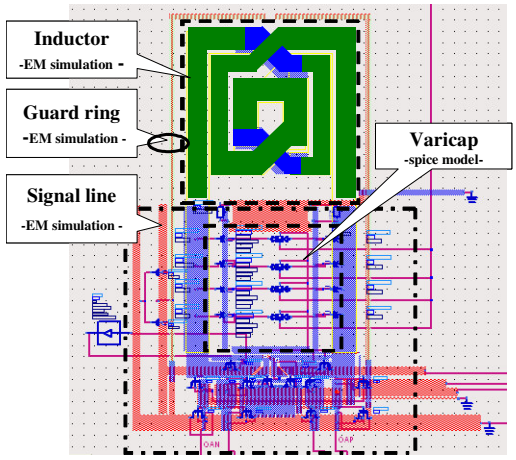

Fig. 10. EM-Co-Simulation setup of 2GHz CMOS VCO.

The setup of EM-Co-simulation is shown in the fig.10. The layout data corresponding to the dotted area in the fig.9 was analyzed by the Momentum simulation. The layout data consists of all the signal lines, inductor, guard-ring.

In ADS schematic, layout component , transistors and other components are correctly connected and 7 tone harmonic balance simulation was done.

Simulation results for the two cases are summarized in Fig. 11. The frequency deviation in "Case1" ranged between 330MHz and 400MHz in the whole rage of control voltage .Approximate frequency error is 16%-18%. In "Case 2 ", the deviation has been drastically decreased to 3MHz in the whole range. Thus, it can be concluded that EM-Co-simulation is accurate and effective for the design of VCO.

The deviation difference between two cases is considered to be the difference of the inductance. This was confirmed by the further Momentum analysis. The resultant inductance in (Case2) was 1.12 nH (a visible increase from the initial estimation of 0.8 nH), which means that the oscillation frequency was decreased by 15%. This increased inductance is ascribed to the parasitic inductances of the "signal lines", and interaction of "guard ring", which is summarized in the fig.10. It can be concluded that the EM-Co-simulation with accurate compact model provides the circuit designer with the accurate prediction of high frequency circuit behaviour.

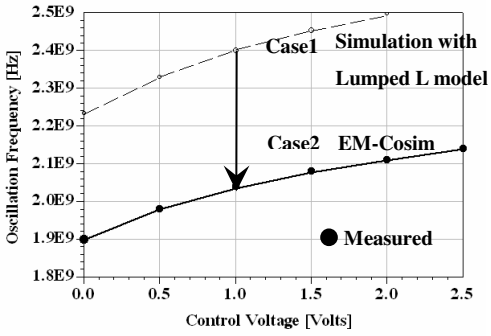

Fig.11 Comparison of the two different setups (case1 and case2) with the measurement data of the RF-CMOS VCO.

IV. Conclusion

An accurate prediction of MOSFETs' operation in the weak-inversion region is becoming very important in the deep-submicron RF-CMOS circuit design. Proper use of both accurate compact model (EKV3.0) and Electro Magnetic simulation is the shortest route to predict the behaviour.

V. Refefences

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