Design tool solutions for mixed-signal/RF circuit design in CMOS nanometer technologies

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Abstract— **The scaling of CMOS technology into the nanometer era enables the fabrication of highly integrated systems, which increasingly contain analog and/or RF parts. However, scaling into the nanometer era also brings problems of leakage power, increasing variability and degradation, reducing supply voltages and worsening signal integrity conditions, all this in combination with tightening time-to-market constraints. Design methodologies and tools need to be developed to address these problems. This invited paper describes progress in modeling techniques for design and verification of complex integrated systems, in circuit and yield optimization tools for analog/RF circuits, as well as in signal integrity analysis methods such as EMC/EMI analysis.**

1 Introduction

The evolution towards nanometer CMOS technologies (90 nm, 65 nm, and below) [1] enables the design of complex Systems on a Chip (SoC) in consumer-market applications such as telecom (e.g. wireless) and multimedia. Such integrated systems are increasingly mixed-signal in nature, embedding high-performance analog or mixed-signal blocks and possibly sensitive RF frontends together with complex digital circuitry (multiple processors, some logic blocks, and several large memory blocks) on the same chip. Fig. 1 shows the growing percentage of SoC designs that contain analog circuits. Integrating the analog/RF parts together with the digital circuitry on a single die allows reducing the overall system cost and power, and improves the overall system performance. Other applications require the integration of passives or sensors and move towards integrated Systems in a Package (SiP) as the most economical solution.

The use of advanced CMOS nanometer technologies however also brings along significant challenges for circuit design (both analog and digital) such as :

- the advent of no longer negligible leakage currents and the impact of power on digital designs;
- the increase in variability of technological parameters;
- dropping supply voltages, that shrink the headroom for analog circuit designs;
- the use of novel devices like FinFETs, and novel materials like high-k dielectrics;
- the surge of novel degradation mechanisms and increasing reliability constraints such as EMC/EMI regulations.

To address these problems, new design methodologies and tools are needed. Unfortunately, EDA tool support for analog and mixed-signal design has strongly been lagging behind its digital counterpart, with the basic tools being used by designers for a long time limited to a schematic capture tool, the universal SPICE circuit simulator and an interactive layout editing environment with some parameterized device layout generators and some verification software [2]. When designing complex integrated systems on chip, this situation is no longer feasible. In addition, integrating analog and digital circuits on the same die creates additional problems of crosstalk and signal integrity, which require tool support for modeling and analysis. This paper will therefore present a brief overview of the current state of the art in mixed-signal EDA tools for modeling, circuit and yield optimization and signal integrity analysis.

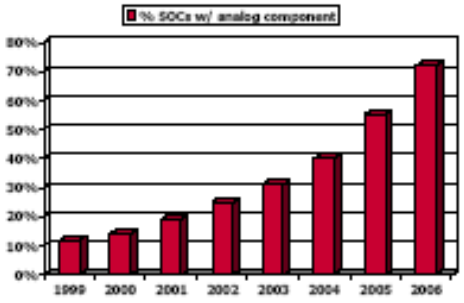

Fig. 1. A growing percentage of SoC designs contains analog components.

This paper is organized as follows. Section 2 discusses progress in circuit modeling techniques, both for top-down design and system verification. Section 3 describes progress in analog/RF circuit sizing and yield optimization. Also hierarchical sizing approaches for more complex designs are presented. Section 4 describes methods for signal integrity analysis, such as the analysis of substrate noise couplings in mixed-signal ICs and EMC/EMI analysis. Finally, conclusions are drawn in section 5.

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2 CIRCUIT MODELING TECHNIQUES

In order to manage the design complexity of mixed-signal systems integratable on a single die today, designers need to adopt different methodologies for design and verification. Design of such systems requires more system-oriented top-down design methodologies, where system architectural explorations are performed at higher levels in the design hierarchy before starting detailed circuit implementations [2,3]. This results in more optimal overall system solutions, catches design errors early in the design cycle and avoids problems at the interface between different blocks (e.g. at the analog-digital interface). The methodology however does require a significant investment from the design team, especially in terms of high-level modeling and setting up a sufficient model library for the targeted application. To generate realistic results, it is important that the high-level models include effects such as dominant nonidealities and parasitic effects (e.g. mismatch) to the extent possible.

An even larger problem in industry today is the verification problem of large mixed-signal systems. The CPU time of a circuit simulator like SPICE increases rapidly with the size of the circuit. Therefore, simulating the entire system at transistor level in SPICE is infeasible. The need has therefore arisen to replace the analog circuits by higher-level models (macromodels or behavioral models) which allow to verify the entire system in acceptable CPU times, at the expense of some (small) loss in accuracy of the simulation results [4]. Obviously, one can trade off accuracy for computation time of the models, and therefore still use more accurate models for the critical blocks, while using more crude but faster models for the other blocks. In such high-level models the circuits are no longer modeled with their structural netlist of individual devices but in a more abstract mathematical way by their input-output behavior, e.g. as a set of parameterized equations.

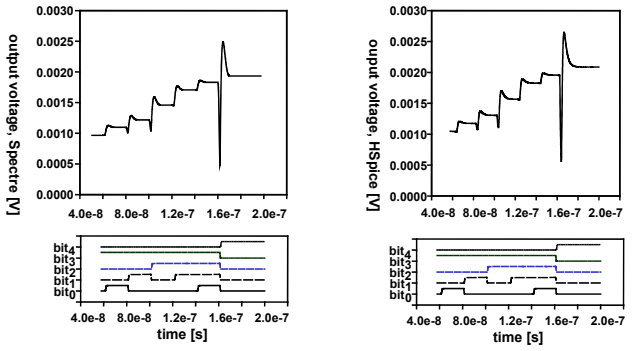

Fig. 2. Comparison between the device-level simulation results (on the right) and the response of the behavioral model extracted from the circuit (on the left) [5].

Example. For example, the dynamic behavior (including finite settling and glitch behavior) of a current-steering digital-to-analog converter (DAC) can easily be described by the following equation [5] where parameters like A_{gl}, t_0 and t_{gl} need to be determined from the underlying circuit implementation, e.g. by regression fitting the model to simulation results of the real DAC circuit at hand :

$$i_{out} = A_{gl}\sin\left(\frac{2\pi}{t_{gl}}(t-t_0)\right)\exp\left(-sign(t-t_0)\frac{2\pi}{t_{gl}}(t-t_0)\right)+ \frac{level_{i+1}-level_i}{2}\tanh\left(\frac{2\pi}{t_{gl}}(t-t_0)\right)+\frac{level_{i+1}+level_i}{2} \quad (1)$$

Fig. 2 then compares the response of the behavioral model (with parameter values extracted from SPICE simulations) with the SPICE simulation results of the original circuit. The speed-up in CPU time is a factor 874 (!!) while the error between the two responses is below 1% [5].

The industrial use of analog higher-level modeling is today enabled by the availability of standardized mixed-signal hardware description languages such as VHDL-AMS and Verilog-AMS, both of which are extensions of the corresponding digital hardware description languages, and both of which are supported by commercial simulators today.

One of the largest problems today is the lack of systematic methods to create good analog behavioral or macromodels – a skill not yet mastered by the majority of analog designers – as well as the lack of any tools to automate this process. Fortunately, in recent years research has started to develop methods that can automatically create such models. They can be classified as follows [6].

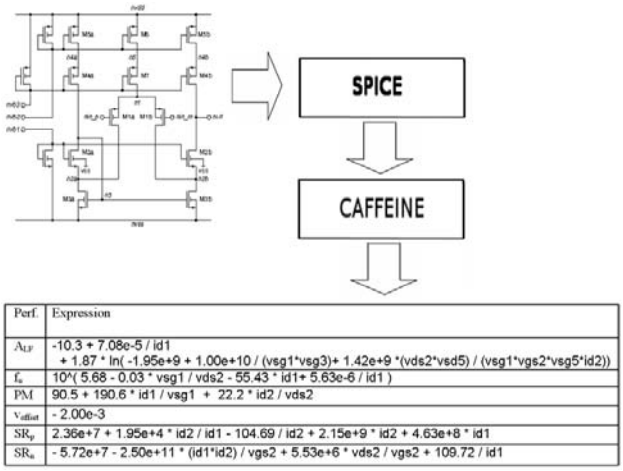

Fig. 3. Basic flow of model generation with CAFFEINE [11] that mines SPICE simulation data to produce template-free models.

- In the *fitting or regression approaches* a parameterized mathematical model is proposed by the model developer and the values of the parameters $\boldsymbol{p}$ are selected as to best approximate the simulated circuit behavior, for instance by minimizing the error between the responses of the real circuit and of the model :

$$error = \int_0^T \left\| v_{out,real}(t) - v_{out,\mathrm{model}}(t) \right\|^2 dt \quad (2)$$

The most critical step is the selection of the model structure or template. Some of the more common templates include polynomials, rational functions,

posynomials [7], neural networks and recently also techniques from data mining [8] and kernel forms such as support vector machines [9,10]. Several companies offer libraries of templates for the most common blocks. However, finding a good starting template in general is not always trivial. Template-free approaches that do not require such a-priori template but generate it as part of the optimization procedure itself have therefore been developed in recent years. The CAFFEINE tool [11] for instance uses genetic programming to evolve a state space model that best fits the SPICE simulation data. Fig. 3 illustrates the CAFFEINE flow for the generation of circuit performance models, i.e. models that relate performance characteristics to design variables, as needed in circuit sizing. Note that in any case the data set used to fit the behavioral model must exercise all possible operating modes of the circuit.

- The *model order reduction methods* are mathematical techniques that generate a simplified model (e.g. a state space model of lower order_ for a given circuit by direct manipulation of its detailed, low-level description [6]. These reduced-order models simulate much more efficiently, while approximating the exact response, for example matching the original model closely up to some specified frequency. Originally developed to reduce the complexity of linear interconnect networks for timing analysis, similar techniques have also been extended to create reduced-order macromodels for linear and weakly nonlinear analog/RF circuits [12,13,14], while current research focuses on methods to model more strongly nonlinear circuits [15,16]. See for example Fig. 4 for a comparison of the simulation results of a phase-locked loop and its linear and nonlinear macromodel [17].

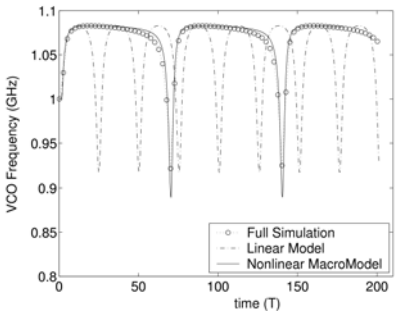

Fig. 4. Comparison between the responses of the original SPICE circuit and of the linear and nonlinear macromodel for a phase-locked loop [17].

Despite the progress made so far, still more research in the area of automatic or systematic behavioral model generation or model order reduction is certainly needed.

3 ANALOG CIRCUIT SYNTHESIS

The traditional analog design flow is very much based on the capture-simulate-analyze loop. This highly manual approach is increasingly at odds with the tight constraints posed by today's SoC or SiP designs. More automated analog circuit design is therefore becoming a viable solution to increase design productivity. Over the past decade, analog design automation has progressed to the point where there are industrially useful and commercially available tools at the cell level – tools for analog circuits with 10-100 devices [2]. Automated techniques for device sizing, for layout, and for basic statistical centering have been successfully deployed.

Analog synthesis consists of two major steps: (1) circuit synthesis followed by (2) layout synthesis. Most of the basic techniques in both circuit and layout synthesis rely on powerful numerical optimization engines coupled to "evaluation engines" that qualify the merit of some evolving analog circuit or layout candidate [2]. The goal of analog circuit synthesis is to create a sized circuit schematic from given circuit specifications. It is a difficult and critical step in the design flow since most analog designs require a custom optimized design and the design problem is typically underconstrained with many degrees of freedom and with many (often conflicting) performance requirements to be taken into account. Typical optimization algorithms used are simulated annealing and genetic or evolutionary algorithms. Another recent trend is the move towards multi-objective optimization [18], which generates a set of design solutions, spread over the Pareto-optimal trade-off hyperfront, so that designers can a posteriori decide on the final design point taken instead of entering a priori weighting coefficients to a lumped cost function. A few noteworthy example circuit synthesis tools include AMGIE [19], ANACONDA [20], and FRIDGE [21], among several others. Some of these underlying techniques have been incorporated in commercial circuit sizing tools that are offered on the marketplace today.

Fig. 5. Multi–objective bottom–up methodology maps design points to performance points via performance simulation. It then propagates trade-offs upwards where they combine to make the next level's optimal design space [23].

For more complex analog systems, like a phase-locked loop, a data converter or an entire RF frontend, such optimization flow at transistor level is prohibitive, since even one iteration already requires too much CPU time. Hence, an hierarchical approach has to be adopted with different levels of design abstraction. The design flow can then proceed in a top-down manner where at each level in the design hierarchy optimization techniques are used to determine the performance specifications of the subblocks within the selected block architecture from the block's overall specifications. This process is repeated down the hierarchy until the device level is reached and all devices have been sized [2]. A tool like DAISY [22] for example performs the high-level optimization of ΔΣ modulators in this way.

An alternative approach presented recently is to use a multi-objective bottom-up synthesis methodology where the hierarchy is traversed in a bottom-up way as shown in Fig. 5 [23]. For all subblocks the Pareto trade-off fronts of their performance space are constructed. These are then used to construct the optimal Pareto fronts of the next blocks up the hierarchy. This process is repeated up the hierarchy until the optimal top–level trade-off is obtained, from which the final design solution can be picked. In the example of Fig. 5, first the trade-off curves for the individual circuits are generated (the SR-GBW trade-off is depicted in the figure), which are then combined to generate the trade-offs (e.g. SNR versus power) at the higher level.

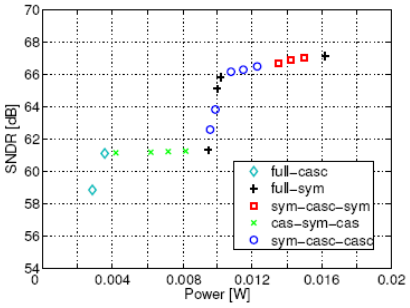

Fig. 6. Trade-off curve of SNDR versus power for a continuous-time Δ-Σ modulator for different topologies of the integrator circuits [24].

In [24] this hierarchical methodology is extended to include different topologies for all circuits at the different levels. Hence building block topology selection is integrated with the sizing at all levels. The methodology provides a system-level Pareto-optimal performance trade-off, where only the topology combinations that effectively generate results at the Pareto front are included. Fig. 7 gives such an example Pareto front for a high-speed Δ-Σ A/D converter designed for the 802.11a/b/g WLAN standard. It can be seen that different lower-level topologies cover different parts of the Pareto front of the SNDR versus power trade-off.

4 YIELD AND MISMATCH TOOLS FOR PROCESS VARIABILITY

Industrial design practice not only calls for fully optimized *nominal* design solutions, but also requires high robustness and yield in the light of varying operating conditions (supply voltage or temperature variations) and statistical manufacturing tolerances (inter-die variations) and mismatches (intra-die variations). With technology scaling these process variations become relatively more important. Physical phenomena responsible for this include the increasingly discrete nature of dopant numbers, line edge roughness, etc.

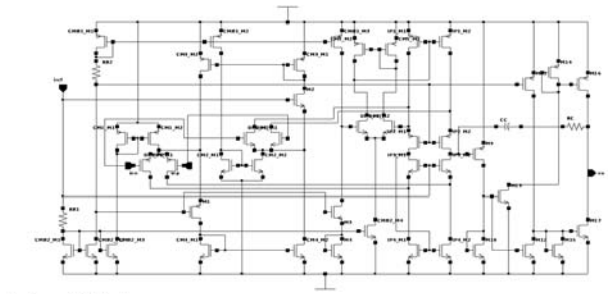

Fig. 7. Amplifier and corresponding response model for Cpk as generated by the CAFFEINE tool ($rmse_{test}$ = 6.3%) [26].

Due to these process-induced variations, the device parameters and consequently also the circuit performance characteristics will show fluctuations. The corresponding parametric yield is the ratio of the number of acceptable (i.e. functional and meeting all specifications) to all fabricated IC samples. The yield of course depends on the nominal design point chosen for the circuit. Estimating this yield is a time-consuming task, which in practice is often performed by Monte-Carlo simulations. An overview of more efficient yield analysis techniques that trade off accuracy versus CPU time can be found in [25]. Most noteworthy are the response surface methods that first generate a model of the circuit performances as a function of the process parameters around the nominal design point, and then use this model to estimate the yield. Fig. 7 shows such response model for the Cpk ("process capability") of a 50-transistor amplifier having 68 design variables, generated with the CAFFEINE tool [26]. This model can subsequently be used for yield optimization.

Current practice to optimize yield is to perform design centering after the nominal design point has been generated first. The design point is then shifted locally to improve the yield. When using a more automated and time-consuming synthesis approach, this two-step procedure however does not make sense, and yield and Cpk optimization should be fully integrated in the circuit synthesis process itself. The most pragmatic solution to do this is to evaluate the circuit performance not only in the nominal design point, but also in a set of predefined worst-case (P,V,T)-corners. The circuit then needs to satisfy the specifications in all corners. The problem with this approach is that the CPU time increases with the number of corners that needs to be simulated and that the number of corners becomes quite large in nanometer

technologies. In addition, not for all analog performance characteristics the worst-case point can be found on some corner. Corner-based design also easily leads to overly pessimistic worst-case design, as shown in Fig. 8.

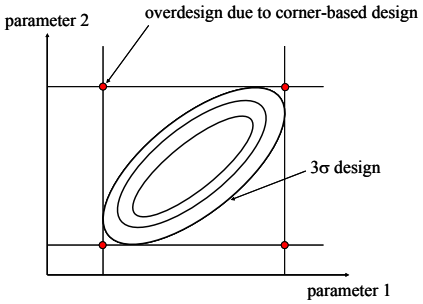

Fig. 8. Difference between corner-based and statistical design against process variability.

Hence, the current trend is to move towards true statistical yield optimization, where the statistical distribution of the parameter variations is considered. Performing a full Monte-Carlo analysis at each optimization iteration is however prohibitive, hence the use of faster methods like response surface modeling (see Fig. 7 as an example). Other recent work uses cell-level synthesis to built statistical trade-off curves that "guarantee" some prescribed yield level for a given performance level [27]. Approximate Monte-Carlo methods help computing the yield efficiently, so that the yield Pareto curves are generated at about 6 times the cost of nominal runs. Fig. 9 shows such statistical Pareto curves for a ring oscillator VCO. An alternative method for yield optimization is the Wicked approach [28] that uses worst-case parameter distances as robustness objectives to obtain a nominal design that satisfies all specifications with as much safety margin as possible for process variations.

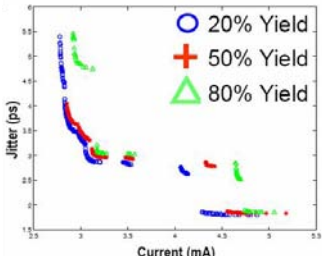

Fig. 9. Statistical trade-off curves showing performance trade-offs for a guaranteed yield level [27].

The field of circuit synthesis incorporating the statistical process variations is still in full progress and more research is needed to develop techniques that can directly synthesize optimal and robust analog designs in an efficient way.

5 MIXED-SIGNAL SIGNAL INTEGRITY

A difficult problem in mixed-signal IC designs, where sensitive analog and RF circuits are integrated on the same die with large digital circuitry, is signal integrity analysis, i.e. the verification of all unwanted signal interactions through crosstalk or couplings at the system level that can cause parametric malfunctioning of the chip. Parasitic signals are generated (e.g. digital switching noise) and coupled into the signal of interest, degrading or even destroying the performance of the analog/RF circuitry. These interactions can come from capacitive or (at higher frequencies) inductive crosstalk, from supply line or substrate couplings, from thermal interactions, from coupling through the package, from electromagnetic interference (EMC/EMI), etc.

Especially the analysis of digital switching noise that propagates through the substrate shared by the analog and digital circuits has received much attention in recent years [29]. At the instants of switching, digital circuitry can inject spiky signals into the substrate, which then will propagate to and be picked up by the sensitive analog/RF circuits. As an example, the SWAN methodology determines the switching noise that is generated by the digital circuits in a system, by a-priori characterizing every cell in a digital standard cell library with a macromodel that includes the current injected in the substrate due to an input transition, and then calculating the total injection of a complex system by combining the contributions of all switching cells over time depending on the event information obtained from a VHDL simulation of the system [30].

In future nanometer technologies, also other signal integrity problems will show up that need to be analysed and modeled. The widespread use of wireless applications creates more and more electromagnetic disturbance signals. To avoid interference problems more and more stringent EMC/EMI regulations are introduced at system, board and even IC level. Safety-critical applications like automotive are taking the lead, but other fields are following. Hence, circuits and systems must be made robust against EM interference, and tools need to be developed to predict efficiently 1) the EM susceptibility of a circuit, and 2) the EM emission spectrum of a circuit. It is important for designers to spot any potential problems early in the design flow.

One of the major problems due to EMI is the change of the DC operating point of a circuit due to rectification effects by nonlinear components (sometimes also referred to as "charge pumping"). Traditional small-signal AC analysis cannot fully reveal this problem, hence other methods are needed. Full transient analysis is possible but is time consuming for different EMI amplitudes and frequencies. In [31] a method is presented that can predict this operating point shift problem in a very efficient way, as a function of the frequency and amplitude of the EMI disturbance. It exhibits a much lower time complexity than transient analysis. The method also gives an indication of the main device(s) that cause this rectification. Hence, the tool can be used to pinpoint weak spots in the circuit design, allowing the designer to correct the problem at an early stage in the design flow.

Example. Fig. 10 shows a LIN driver circuit as used to drive the single-wire LIN bus used in cars. The long wiring in a car makes the system extremely susceptible to conducted interference. In a LIN driver bits are encoded as the delay

between a rising and a falling edge on the LIN bus. For this reason, it is important that the slope can be controlled accurately and is constant during transition. Fig. 10a shows a simple implementation: the two current sources are switched on/off periodically to obtain a constant slope. Though this circuit performs well in ideal circumstances, the output stage is very sensitive to EMI injection at the LIN output, which causes charge pumping over the parasitic feedback capacitor C_s which will alter the slope of the signal. Fig. 10b plots the DC shift as a function of the EMI frequency and shows a good agreement between the results of the much faster EMI analysis tool and those of the full transient simulations.

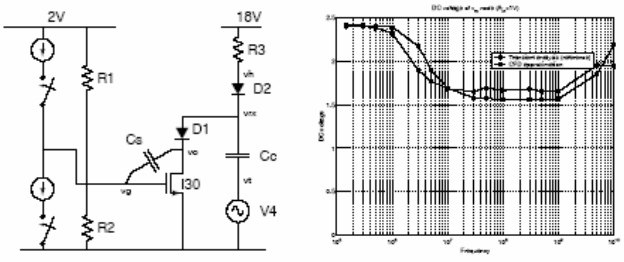

Fig. 10. (a) Principle schematic of a LIN driver, and (b) simulated dc voltage at the output as a function of the EMI frequency, indicating the EMI-induced dc shift.

6 Conclusions

The last few years have seen significant advances in both design methodology and CAD tool support for analog, mixed-signal and RF designs, enabling the design of mixed-signal integrated systems on chip in nanometer CMOS technologies. Analog behavioral modeling enables top-down design flows and allows the verification of complex mixed-signal designs before tape-out. Analog synthesis tools based on powerful optimization methods have appeared on the market. Efficient yield analysis and optimization methods are being developed to cope with increasing variability. And many tools are being developed to analyse signal integrity in mixed-signal ICs, such as due to substrate and supply noise couplings or due to electromagnetic interference (EMC/EMI).

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