DFM/DFY practices during physical designs for timing, signal integrity, and power

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Abstract - **We present our experience of DFM (Design for Manufacturability) and DFY (Design for Yield) considerations on physical designs at 0.13um and below technology nodes. The impact of some DFM approaches on timing and signal integrity are addressed. We also present our experience of yield analysis and improvement for the designs with process variation and dynamic IR drop issues.**

I Introduction

As VLSI technology continues to advance towards nanometer dimensions, current design methodologies from architecture to tape-out are greatly challenged. Deep sub-micron physical effects make it difficult to reach design closure for timing, signal integrity, and low power, and deep sub-wavelength lithography limitations also must be overcome to reach manufacturing closure. For example, as process dimensions scale down to 65-nm and below, the shape of a metal wire can vary depending on the spacing between the wire and the surrounding metal polygons [9]. Design closure and manufacturing closure have made the turn-around-time to tape-out longer, and the corresponding potential defects also make the yield getting lower at 0.13um and below technology nodes.

To achieve profitable yield, advanced design processes are being developed to make sure that the chip can be correctly manufactured with the smallest possible dimensions, and the process variation of device and interconnect can be well taken into account during chip implementation. Such methodology is also called design for manufacturing (DFM), or design for yield (DFY).

Chip defects commonly are classified into three types: random defects, systematic defects, and parametric defects. Random defects are typically associated with random particles and result in open/short, resistive pinching, and added coupling. Systematic defects are related to design process technology such as the chemical impact on process materials or the mechanical impact on manufacturing/lithographic processes, etc, which cause planarity, antenna effects, via opens, and various other effects. Parametric defects refer to the fact that a chip may perform its logical function correctly, but the process variations of devices and interconnects will result in timing, signal integrity, and power bus voltage-drop to differ from specification.

In this paper, we review current state-of-the-art methods to address current DFM challenges, and represent various techniques for yield improvement in Section II. We will discuss our experience on improving manufacturability and yield for random, systematic and parametric defects, especially for defects due to dynamic IR drop at 130nm/90nm nodes in Section III. Finally the conclusions are given in Section IV.

II. Prior Art

The future of improving manufacturability and yield can be seen in next generation of electrically aware EDA tools. Some manufacturing process effects should be taken into consideration at the early design stage, when driving power and timing requirements are considered. In this section we provide a brief overview of the recent progress in these areas.

A comprehensive yield optimization throughout the design flow should cover:

A. Yield Optimization with Cell Mapping

A cell layout may be characterized with a "yield view" or "yield cost" that captures its impact on yield [5]. In general, a cell design with the same functionality may have different layouts with different "yield costs". For example, the same cell may have a seven-track layout or a five-track layout. For a given process, a "higher-yield" library can be created by designing a "higher-yield" cell for each cell in the library.

B. Yield Optimization during Chip Prototyping

The primary benefit of being able to estimate yield is that yield information can be made available in the early design phase. Chip prototyping is a powerful way to quickly achieve design closure on area, timing, and power. At the prototyping stage, power planning, cell placement, row utilization, trial routing, etc., may be analyzed and evaluated to get a design with good yield by comparing one floorplan against another.

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C. Yield Optimization during Routing

Routing is a key design stage for yield improvement. Many techniques are carried out at this stage. They include:

- Critical area analysis (CAA) driven wire spreading/widening, redundant via insertion and recommended end-of-line extensions
- Virtual chemical mechanical polishing (VCMP) driven metal fill and RC extraction
- Lithography process check (LPC) aware routing

CAA uses technology-specific data from a yield parameter file supplied by semiconductor manufacturing foundry. It measures the sensitivity of a layout to the problems caused by random particles falling on the wafer during processing, which may cause open or short failures. It enables us to estimate the random particle defect related yield loss, and also helps to identify problem spots on the design from yield perspective. For example, CAA identifies random manufacturing defects caused by conducting or non-conducting particles and drives wire spreading and wire widening corrective actions. Via replacement can also improve yield on vias. Wire spreading combined with double-cut via has been proven to improve total yield results.

VCMP analysis identifies metal and dielectric thickness variation hot spots, and guides dummy metal insertion to improve thickness uniformity throughout the chip.

Additionally, lithography simulation eliminates hot spots and ensures LPC correctness seasonably. Recently, physical design methods, such as Post-RET Verification (PRV) and DFM in Layout-to-silicon-pattern Transfer (DFP), are proposed to permit designers to predict and compensate for optical proximity, phase shift mask and other distortions that are introduced at the very last stages of manufacturing.

D. Yield Improvement on Testing

It is well known that power consumption during test mode is usually higher than that during functional operation [6]. The power consumption during test mode tends to dominate functional power consumption due to the increased switching density during scan shift and scan capture (the functional portion of a scan pattern). In general, test-mode toggle activity is typically higher than normal functional activity. Therefore, test mode can be used to represent the worst-case scenario for dynamic IR drop.

Dynamic IR drops may induce performance degradation of standard cells and thus result in setup/hold time violations. Usually, scan pattern on tester is used to screen out the chips with manufacturing faults. However, due to dynamic IR drop issues, it is very likely to overkill those chips that have no manufacturing faults and pass function mode test but failed at test mode test.

Dynamic IR analysis thus becomes very important for 0.13um and below designs. For today's designs, both static and dynamic analysis should be utilized from initial floorplaning (power planning) throughout the design flow. In conventional design flows, decoupling capacitance (decap) cells are inserted intentionally between power and ground buses to remove dynamic IR drop that arise from resistive and inductive effects. One popular approach for adding the additional capacitance is to swap filler cells with the decap cells. If cell swapping does not provide enough decap cells, major changes on the implementation may be needed to add the required decap cells.

III. Experience Sharing

DFM concept has been raised for many years since 0.13um technology node. However, most of the EDA tools only focus on OPC (Optical Proximity Correction) at that time. As design process have continued to shrink to 90nm and 65nm, CAA, CMP and LPC effects are no longer ignored and need to be taken into account during physical design phase. EDA vendors thus put many resources to develop related tools for analysis. In this section, we will present our experience of DFM analysis on 65nm designs and also show how we do yield analysis and improvement for some projects.

A. CAA Analysis

By analyzing the critical areas, defect-limited yield can be estimated based on the probability of the failures of the cells, vias, and point defects on routing. These failures can then be prevented during the design stage by spreading wires evenly, widening the wires, and adding redundant vias.

Wire spreading is an effective approach to reduce critical area and also the potential of short circuits. Wire widening, on the contrary, may increase the critical area, but it can reduce the potentials of open circuit effectively. Wire spreading helps not only yield but also signal integrity (SI) and timing. However, wire widening improves only yield and may have impact on timing, SI, and power. To have further improvement of yield, redundant via insertion and dummy metal insertion are needed in the design flow.

Table-1 illustrates the impact of double cut via insertion on yield. After replacing around 34% 1-cut via (single via) with 2-cut via (double via), the yield loss due to via defect (Y1) is reduced around 0.14%. This yield improvement of course is based on random defect point of view. The 0.14% actually is not significant improvement, but we usually replace the double vias as many as possible because from systematic mechanisms (pattern dependencies in the layout) point of view, a second via disperses localized effects and limits the probability of a failure.

Table-1 Yield improvement by adding redundant via

	1-cut via#	2-cut via#	Y1	Y2	Y3
w/o double via	5.33E+06	3.25E+03	0.712%	0.305%	1.015%
w/i double via	3.51E+06	1.82E+06	0.571%	0.314%	0.883%

*Y1: Yeild lost% due to via defect
*Y2: Yield lost% due to wire defect
*Y3: Total yield lost%

B. VCMP to Timing Impact

Chemical Mechanical Polishing (CMP) simulation is a key enabling process for planarization and patterning copper interconnects in the deep sub-micron IC fabrication [1]. Layout pattern variation, which may result in metal dishing and oxide erosion, often decreases chip yield and degrades circuit performance.

To take the CMP effect into account during RC extraction, some foundries have developed DFM related data kits, e.g., TSMC's DDK (DFM Data Kit) and provide them to customer for VCMP simulation. VCMP simulation may analyze the metal and oxide thickness of the design by referring to the DDK parameters. To examine the timing impact due to CMP effect, we did an experiment on a 65nm design. We did RC extraction twice, one using original RC extraction flow, and the other one using VCMP simulation with encrypted DDK model. As the results illustrated in Fig-1, the timing of considering VCMP simulation may has around 4.5% timing difference with compared to that without considering VCMP simulation.

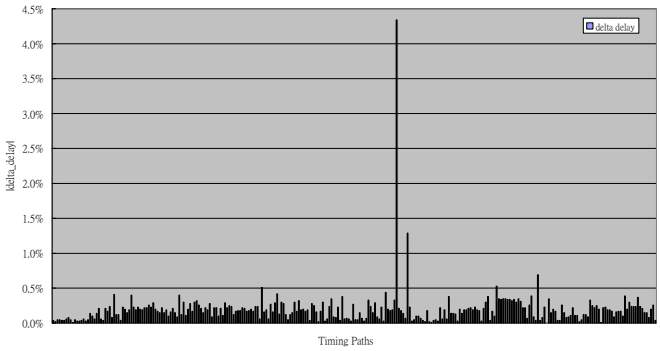

Fig-1 The timing comparison of RC extraction with and without VCMP simulation.

To minimize the impact of CMP effect, dummy metal fill becomes a practical technique. In real chip designs, the metal density rule is rarely met and is hard to be improved by using manual methods. Therefore, an automatic dummy metal insertion flow is necessary. Virtual CMP simulation can be integrated with the flow to predict metal and layout thickness, insert dummy metal fill and offer more accurate parasitic extraction for better timing accuracy and less margin for process variation. The process of adding dummy metal fill may cause increased coupling capacitance on adjacent wires, which may further impact the timing and SI. As the waveforms shown in Fig.-2, they represent the timing increase of some timing paths after adding dummy metal fills. Usually, the timing path delay after considering the coupling capacitance of dummy metals is bigger than original delay without considering dummy metal. In Fig.-2, it shows the timing difference may be around 3.5%. In Fig-2, we also show the timing difference between considering VCMP simulation and not considering VCMP simulation. Most of the differences are within 0.5%.

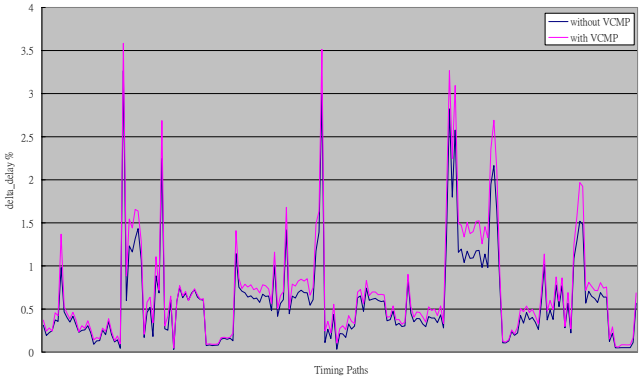

Fig-2 Timing impact due to dummy metal fills

Fig.-3 shows the impact of SI incremental delay due to dummy metal fills. The results show that the SI incremental delays of some timing paths may have 1.5 times increase and some paths may have 20% decrease.

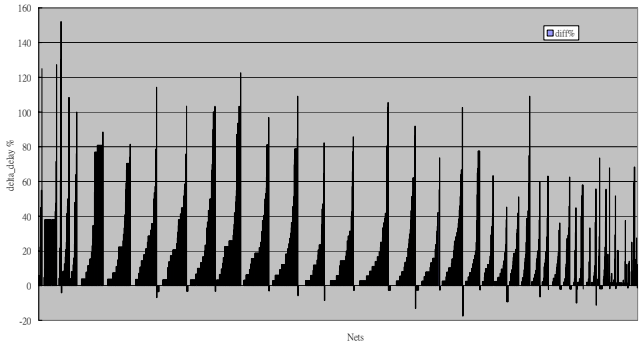

Fig-3 SI timing impact due to dummy metal fills

C. Dynamic IR Prevention & Verification

In addition to CAA for random defects and VCMP for systematic defects, we would like to share our experience of dynamic IR drop effects for parametric defects.

In a real case, low frequency scan stuck-at patterns passed all test conditions during manufacturing test, while scan transition patterns failed at worst corner voltage. Such phenomenon was presumed to be caused by either excessive IR drop or crosstalk problems, resulting in unacceptable

delays during the high speed scan transition capture operations. Table-2 shows the results of timing checks with voltage drop considerations. Before taking voltage drop into account for timing analysis, both of CASE1 and CASE2 have no timing violation. However, after taking dynamic IR drop into account, there have 51 and over 100 violations paths for CASE1 and CASE2 respectively because of the timing degradation of each cell instance. For this situation, yield may be overkilled if dynamic IR drop is not resolved before tape-out.

Table-2 Timing Checks with IR Drop Consideration

	Average %delta	Min %delta	Max %delta	Worst Slack	#failed paths
CASE 1	0.28%	-0.31%	1.59%	-138.8ps	51
CASE 2	0.41%	-0.09%	0.65%	-117.8ps	> 100

Another experience of yield overkill due to dynamic IR drop for a 0.13um design is as below. For this case, the chips pass all function patterns test on tester and also pass system verification. However, the yield is around 30% due to the failure of scan patterns. After investigating the failures, we found that scan mode hold time violation due to dynamic IR is the root cause. After adjusting test clock delay, improving the power plan and reserving more timing margin for dynamic IR drop, the yield is increased to over 90%.

In practice, it is often too late to resolve dynamic IR hot spots with decap cell insertion by the time when VCD-based analysis is performed. In most cases, there simply is no space at this point for decap cells to be inserted at where dynamic IR hot spots may occur. As illustrated in Fig-4, the improvement in voltage drop may be trivial, even while the number of decap cells inserted is increased dramatically towards 200K instances.

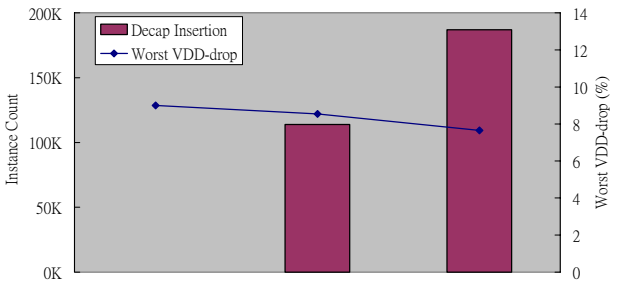

Fig-4 Dynamic IR drop improvement by decap insertion

In this situation, it makes sense to perform dynamic prevention as early as possible in the design flow and reserve the required space for decap insertion up-front, as shown in Fig-5. In this flow, flip-flop density checking flow is developed by GUC and patent pending.

Dynamic IR drop occurs when the simultaneous switching of on-chip components causes a dip or spike in the power/ground grid. These occurrences may reduce the logic gate noise margins and result in functional or timing failures. Flip-flop density checks provides an easy and effective method to identify the hotspots that may induce dynamic IR problems. This is in contrast with the expensive and time consuming VCD-based dynamic IR analysis. In addition, flip-flop density analysis results have been correlated with various designs against state-of-the-art dynamic IR analysis. The experiment results reveal a high correlation between the VCD-based dynamic IR analysis and the flip-flop density check. The auto fix flow with cell padding approach is a scalable, efficient, and low-cost method to improve yield while avoiding switching density too high.

Package loading is another factor that can play a significant role in IR drop transients. Packages add resistance, capacitance and inductance to I/Os. Since this additional loading will affect IR drop, it should be included in dynamic rail analysis.

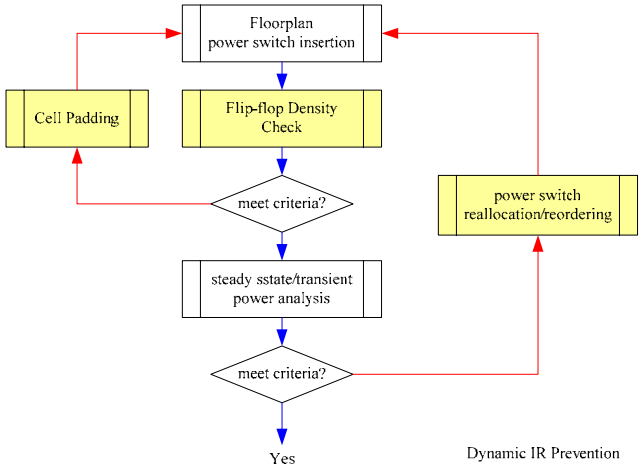

Fig-5 Dynamic-IR prevention during prototyping

D. Wafer Acceptance Test (WAT) Parameter Analysis and Yield Correlation

In order to achieve sustainability in higher-yield production, yield management has emerged as an increased important area, and plays a significant role in technology development and continuous manufacturing process improvements. One important component of yield management is effective yield analysis in order to achieve accurate yield prediction [4]. Effective yield analysis is an integral for driving quality products to the market as quickly as possible with optimal yield output. Rapid data collection and reliable analysis reduces the response time to yield and process problems.

An important aspect of yield analysis is the statistical analysis of yield parameters. Fig-6 illustrates a statistical overview and histogram of the selected lot data, which helps to highlight that the relationship between poly resistance and

yield. Each spot of a dot line indicates the CP-yield of a single lot and the associated fitting curve of those CP-yields is highlighted with a wider dot line. Each ohm value in respect to poly resistance is denoted with a spot of a solid line and its associated fitting curve is highlighted with the narrower dot line. It is obvious that when the ohm value of poly resistance is lower, the CP-yield can be improved from 50 percent to 85 percent.

The poly resistance is actually related to POLY-CO thickness. In this yield trend analysis, the best ohm value of poly resistance is close to '5.75'. Under this condition, the CP-yield could be improved almost up to 90 percent. When we decrease the POLY-CO thickness, e.g., increase of poly resistance, the CP-yield is quite unstable. The yields of memory BIST and scan patterns drop significantly.

The yield analysis shows that the solution of this yield improvement actually has not been covered by current DFM solutions. It is difficult to predict yield even we bring the most advanced and appropriate tools to resolve the issues of manufacturing process effects. The results indicate that some parameters other than those related to CAA, CMP, and LPC may also affect the yield significantly, but they are not well modeled in current DFM tools.

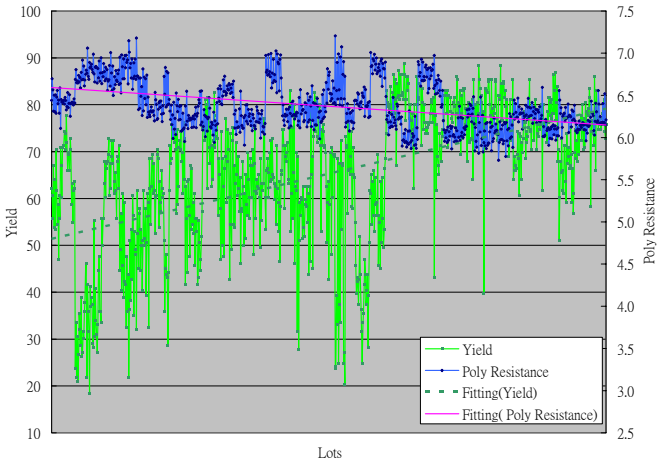

Fig-6 Poly resistance versus CP-Yield analysis

As chip designs are pushed to production faster and faster, and designs become even more complex, yield analysis must be sophisticated enough for engineers in order to fully understand all of the components of yield and defect detection. Once a product is in production, continuous improvement to the process can further increase quality yield output. Thus, robust, reliable numerical algorithms are essential to achieving accurate results from yield analysis efforts. Besides, statistical and visual correlation is an important aspect of yield and failure analysis.

IV Conclusions

Accurate yield analysis increases yield predictability, ensures quick response time to yield problems, and reduces die loss. Thus, having an accurate analysis tool is very critical to making good decisions during design optimization as early as possible.

Our yield trend analysis shows that the analysis of WAT parameters also has great help on yield improvement even under the most careful DFM regulations provided by foundry. The results obtained also indicate that some parameters in WAT other than CAA, CMP, and LPC parameters may impact yield very much as well, but they have not covered by current DFM available tools. There still have a big room for DFM tool development for yield enhancement.

Besides, post-layout yield improvement solutions are less effective and lead to increased design iterations. Inherent limitations of the manufacturing process result in process variations that can cause catastrophic or parametric failures. Rule-based design-for-manufacturability (DFM) solutions are no longer effective at 65-nm and result in "overkill" or pessimistic designs. Ensuring manufacturability and maximizing yield are major challenges in 65-nm designs and it is important to address yield related issues throughout the design flow.

An ideal electrical DFM/DFY solution does not require any changes to existing design flows, does not require a different hand-off to manufacturing, and does not require detailed proprietary process information from the foundry. Thus, chip designers can reap the substantial benefits of electrical DFM/DFY at a very low cost of adoption. To achieve this compliance, DFM/DFY tool accuracy, performance as well as usability all must be verified with massive foundry data, a task that can only be accomplished in collaboration between the foundry and its partners.

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