Modeling Sub-90nm On-Chip Variation Using Monte Carlo Method for DFM

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Abstract - For sub-90nm technology nodes and below, random fluctuations of within-die physical process properties are also known as random on-chip variation (OCV). It impacts on the VLSI/SoC design yields significantly. This paper presents a recent silicon test chip experiment result which uses a set of innovative nanometer test structures and Monte-Carlo-based three-dimensional electromagnetic RC simulations to achieve silicon-correlated corner modeling of OCV that can be applied to the upcoming statistics-based timing analysis (SSTA) for design for manufacturability (DFM). Modeling and correlating OCV based on the randomly varying physical process parameters is therefore achieved for the realistic corner modeling of advanced copper and low-K.

I. INTRODUCTION

Successfully scaling of transistors (front-end of the line, FEOL) and interconnects (back-end of the line, BEOL) in the sub-90nm nodes have been achieved and available for VLSI/SoC designs. It results in the speed-up of the transistors for the benefits of the VLSI/SoC performance but the delay and random variation of interconnects impacts the overall VLSI/SoC product yields and performances more prominently [1].

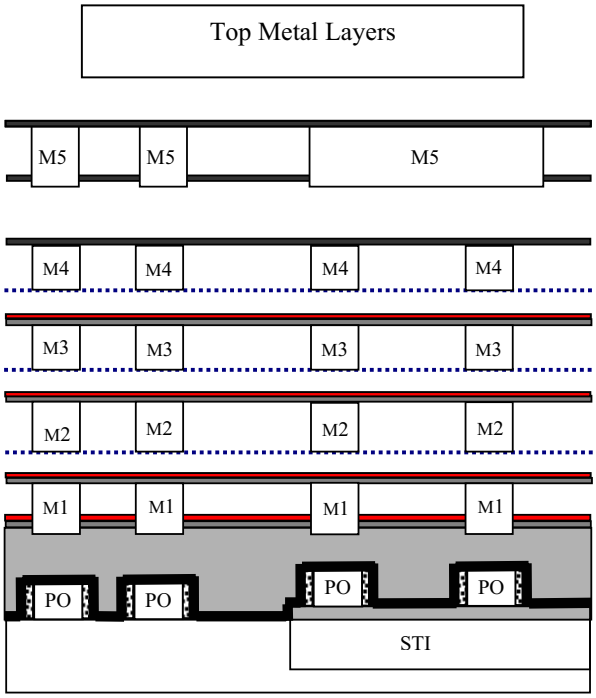

Figure 1. Cross-sectional view of a sub-90nm technology with six or more metal layers.

State-of-the-art sub-90nm VLSI/SoC designs require the BEOL to consist of 6 or more metal layers of copper-alloy interconnects insulated by low-K dielectrics, as shown in Figure 1. Undesired BEOL on-chip variations (OCV) increase with scaled technologies. Therefore, the corresponding interconnect process parameter variations such as metal thickness, metal width, and dielectric thickness must be accurately validated for each metal layer to model the resulting interconnect capacitance and resistance variations.

Figure 2 is a typical 3-dimentional (3D) BEOL electromagnetic-based capacitance simulation [2] [3] with precise thickness and equivalent rectangular CD of three metal lines above a substrate or a ground plane.

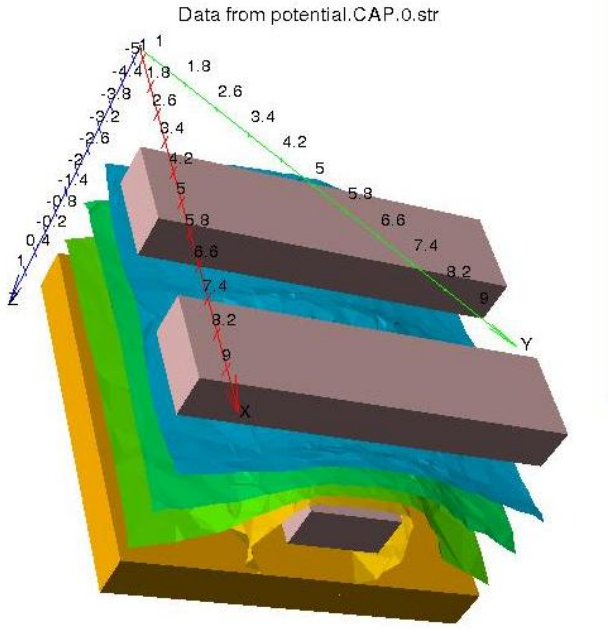

Figure 2. Electromagnetic-based BEOL capacitance simulation of three metal lines above a ground plane.

While the 3D electromagnetic simulations require precise dimensions and material characteristics, the Monte-Carlo method [4] is a numerical simulation of statistically varying inputs to reproduce stochastic variables preserving the specified distributional property outcomes, such as the 3σ (99.7%) shown in Figure 3. The varying dimensions and material characteristics in sub-90nm BEOL OCV can be classified into systematic variations as well as random variations [5]. Systematic OCV has a deterministic pattern-dependent trend and is best to be corrected through OPC, VCMP, and dummy patterns. The emphasis of this paper is on realistic corner modeling of random OCV for copper and low-K. In essence, modeling random

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on-chip variation (OCV) of sub-90nm BEOL requires a statistical validation methodology.

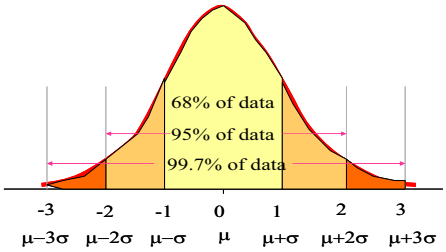

Figure 3. Statistically 3σ BEOL variations cover 99.7%.

A Monte-Carlo-guided RC simulation (MCGRC) is designed with the aforementioned 3σ statistical spread inputs for the batch execution of numerous capacitance and resistance simulations. The output generation is guided by the Monte-Carlo statistics with the resulting example shown in Figure 4, which is to represent the probability distributions of the BEOL performance variation spreads.

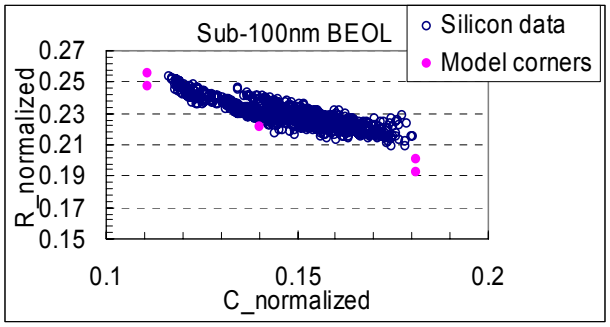

Figure 4. Modeled corners compared with silicon data.

The modeled corners in Figure 4 from our MCGRC indicate the capacitances spread from 0.11 to 0.18 normalized values while the resistances spread from 0.19 to 0.26 normalized values, which closely match the silicon data (depicted in empty dark-colored circles) but the correlation obviously can be improved further. Using more rigorous and more realistic principal variation components, e.g. IMD thickness, Rs, and metal thickness, the silicon data are targeted to be more closely matched through MCGRC. In this way, the process parameter variation data are ready for SSTA-based VLSI timing analysis, signal-integrity analysis, and DFM.

II. Previous Work

Examining recent OCV related articles [5] [6] [7] indicates that they are based on the device or performance variations which are derived from the variance of physical process parameters. On the other hand, we emphasize on using more fundamental and more realistic principal variation components, e.g. IMD thickness, Rs, and metal thickness, as our OCV modeling. In this way, we target the silicon data to be matched with that from the proposed MCGRC method.

Statistical parameter analysis has been used in maintaining accurate worst-case SPICE models for more than one decade [8]. For the statistical analysis on BEOL OCV by other articles [6] [7] [9] [10], they aggregate the random OCV modeling with systematic OCV modeling together without discrimination for SSTA, which can exhibit too big a statistical spread to allow for design convergences. SSTA should be based on random OCV primarily.

Although electromagnetic field simulations [2] [3] of BEOL have been used for resistance and capacitance modeling for decades, we expand them by applying to a Monte-Carlo guided methodology, which carefully selects representative BEOL cases to avoid the slow speed of the field simulation software.

III. Systematic versus Random Variations

Reducing systematic OCV to minimize the overall OCV and design margin has been studied by using (1) wire spreading and widening, (2) virtual chemical mechanical polishing (VCMP) based dummy metal fill for uniform layer and metal thickness, (3) model-based lithography simulation eliminating hot spots and ensuring lithography proximity correctness.

The result is a BEOL topology with reduced systematic OCV, which benefits a lower failure probability. To combat yield loss due to missing, malformed, or resistive vias, redundant vias are inserted by the foundry-recommended tool which selects the most appropriate configuration for the uniform density of the layers of the layout.

In essence, improved quality of BEOL through wire spreading/widening, dummy metal/via insertions, and lithography hot-spot elimination, is believed to accurate parasitic extraction and better timing accuracy with less design margin for process variation.

Focusing the modeling of random OCV, our paper describes how worst-case BEOL models can be derived for sub-90nm CMOS processes for an integrated VLSI/SoC design environment using SSTA.

IV. Monte-Carlo Based Method

Our method starts with carefully selecting representative BEOL cases to avoid the slow speed of the field simulation software. During advanced VLSI/SoC designs, majority of interconnects are densely routed as Figure 5 with conductors above as well as beneath.

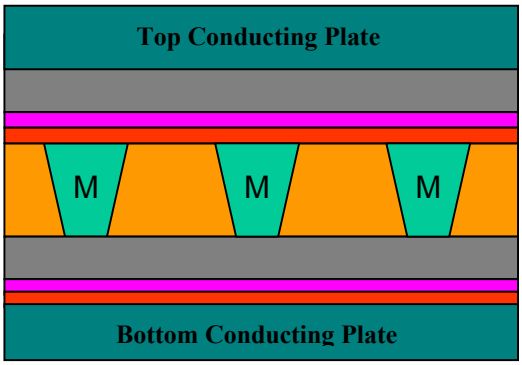

Figure 5. Typical interconnects with metal lines between two conducting plates.

Another typical but irregular "realnets" in advanced chip designs [10] are depicted in Figure 6 where the light-colored metal lines are in a sparser environment, i.e. under dark-colored metal lines instead of a big-area conducting plate. The light-colored and dark-colored metal lines are then routed between two conducting plates with dense grids.

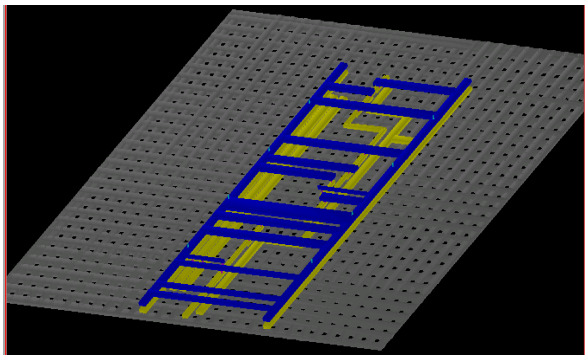

Figure 6. An irregular realnet between grid plates.

The partial cross-sectional view of Figure 6 with the realnet and the metal lines routed between two plates is shown in Figure 7.

Figure 7. A partial cross-sectional view of the light-colored realnet in Figure 6, which is between two grid plates.

Besides using MCGRC field simulations of varying BEOL process parameters for Figure 5 and Figure 6, we add another regular BEOL structures for MCGRC, shown in Figure 8, with metals lines in a sparser environment, i.e. between two non-adjacent conducting plates.

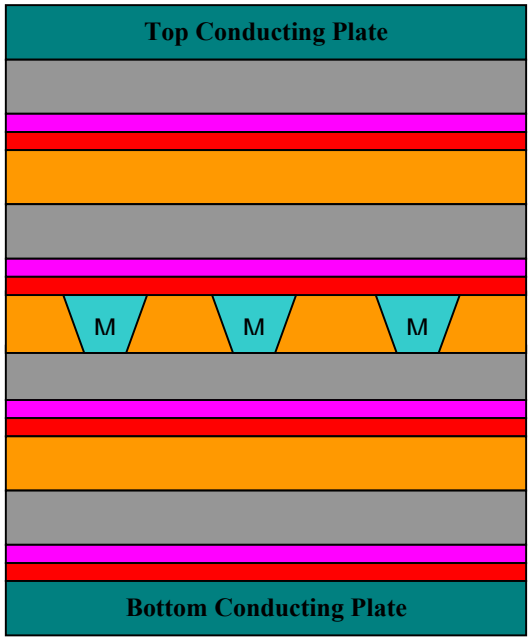

Figure 8. Another typical interconnects between two non-adjacent conducting plates.

For advanced sub-90nm CMOS nodes, the aforementioned three BEOL structures, i.e. Figure 5, Figure 6, and Figure 8, are believed to occur frequently. They represent three density levels of BEOL and can be the typical building blocks of the interconnects of the VLSI products. Using them, we design a Monte-Carlo-guided RC simulation (MCGRC) which requires the mean (μ) and the variance (3σ) statistical process parameter variations of the physical process parameters for the executions of numerous capacitance and resistance simulations guided by the Monte Carlo. Advanced BEOL manufacturing processes, as shown in Figure 1, can consist of dozens of varying process parameters. For the three typical structures in our research, the number of varying process parameters is constrained and can lead to faster Monte Carlo simulations.

Using the dense structure in Figure 5 as an example, its RC performance variance can be affected by the following nine varying process parameters:

1. CD bias;
2. Metal thickness
3. Sheet resistance;
4. Permittivity of Low_K between metal lines;
5. Permittivity of Low_K above metal lines;

6. Thickness of Low_K above metal lines;
7. Permittivity of Low_K below metal lines;
8. Thickness of Low_K below metal lines;
9. Via resistance.

For the structures in Figure 6 and Figure 8, they are sparser than that in Figure 5 and can be affected by three or four additional varying process parameters. If some of the varying process parameters are not independent, the MCGRC requires the interdependency data.

Examining our proposed MCGRC, as depicted in Figure 9, it begins with these three steps: (a) Collecting the raw silicon process parameter variation data, (b) Analyzing and generating BEOL 3σ variations of BEOL process parameters, and (c) Measuring and generating raw silicon RC corner data.

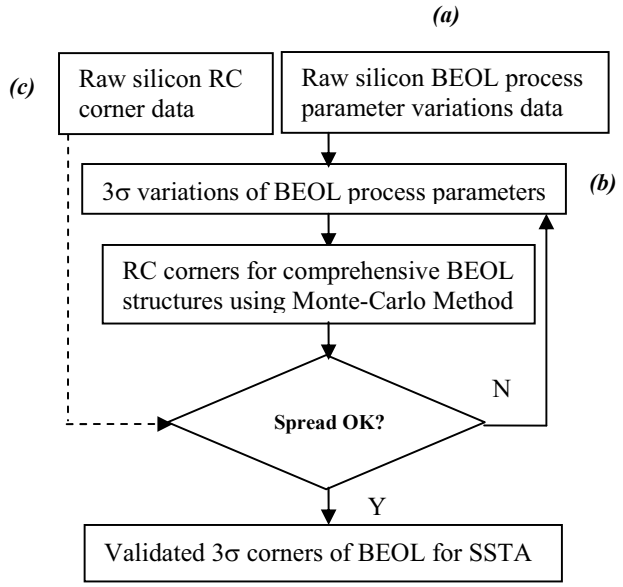

Figure 9. Validating BEOL process variations for SSTA.

In our MCGRC, the principally varying components based on each sub-90nm node's actual manufacturing data should be carefully collected and quantified for our approach to arrive at the best guessed 3σ variations for a comprehensive and efficient execution job of BEOL MCGRC simulations.

The validating step of the MCGRC is depicted at the center of Figure 9, which accepts the RC corners of the MCGRC simulation results and compares the spread with the measured raw silicon BEOL RC corner data. If the two spreads do not match well, the analysis and generation of the 3σ process parameter variations should be conducted again until the two spreads match well with each other.

In Figure 10, an MCGRC execution with 1000 electromagnetic field simulation runs is shown for the dense structure in Figure 5.

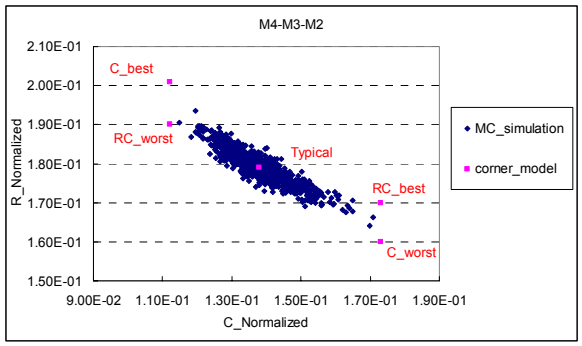

Figure 10. An MCGRC simulation result for M4-M3-M2 dense structure.

Overlapping the MCGRC results with the silicon RC corners in the same figure, the MCGRC simulation results match well with the five silicon RC corner models, i.e. C_best, RC_best, typical, RC_worst, and C_worst.

Depicted in Figure 11 is an MCGRC simulation for the capacitance spread of the realnet in Figure 6. For a set of 926 3D electromagnetic simulation runs, the capacitances spread from 0.3 to 0.37, which is narrower than the silicon capacitance corner of 0.29 to 0.38 but the result is considered satisfactorily matched.

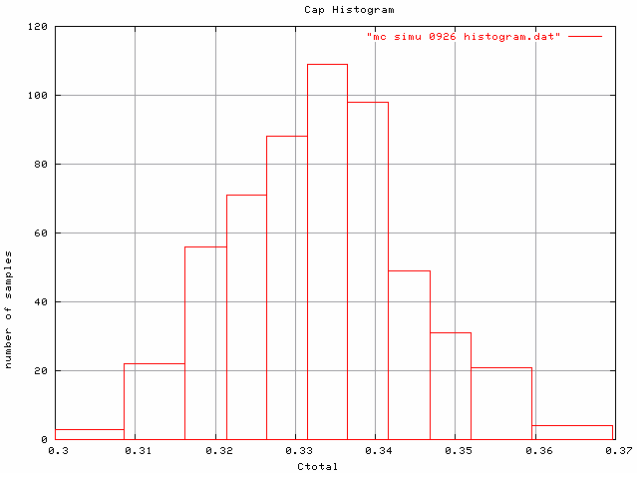

Figure 11. An MCGRC simulation result for a realnet in Figure 6.

As for the MCGRC simulations of the sparsest structure in Figure 8, we arrive at the RC plot of Figure 12 where two sets of silicon corners in lighter colors have been available. The square-shape corner model is based on a recent set of silicon data while the triangle-shape corner model is based on a rigorous set of new silicon data. Exercising the iteration in Figure 9, MCGRC data match better with the new corner model.

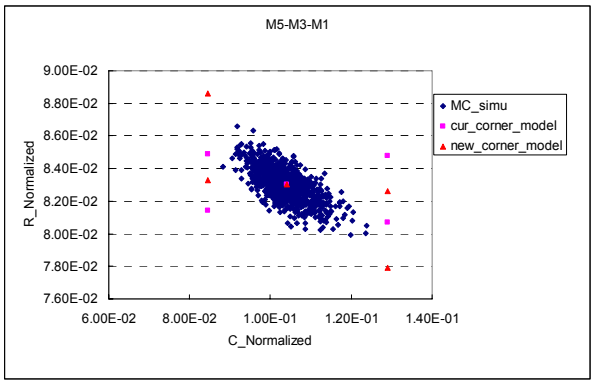

Figure 12. An MCGRC simulation result of the sparsest structure in Figure 8.

VLSI/SoC designs can use all metal layers available from the foundry, so the MCGRC simulations are to be applied by the foundry to each metal layer to come up with a validated technology-dependent 3σ process parameter variation data for the layout parameter extraction (LPE) phase in the corresponding sub-90nm BEOL technolology's SSTA flow, as shown in Figure 13.

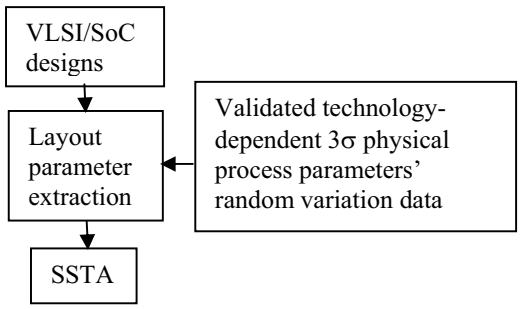

Figure 13. Applying the technology-dependent 3σ process parameter variation data to the SSTA flow.

V. Summary and Future Work

A Monte-Carlo-guided resistance and capacitance simulation (MCGRC) method is proposed and depicted in Figure 9. The uniqueness of our method is in the statistics-based and silicon-verified 3σ physical process parameters' random variation data for the layout parameter extraction (LPE) during SSTA flow.

Based on the flow depicted in Figure 13, SSTA is to perform a statistical look at how each and every FEOL and BEOL device from LPE will operate across the variations in the supplied process parameter variations. The future work is to validate the available statistical static timing analysis (SSTA) algorithms targeting using solid algorithm to work reliably to meet timing, to achieve signal integrity, and to improve parametric yield for DFM.

VI. Acknowledgements

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