Thermal-driven Symmetry Constraint for Analog Layout with CBL Representation

Jiayi Liu
EDA Lab, DCST of Tsinghua University
Beijing, China, 100084
Email: liujiayi@vip.sina.com

Sheqin Dong*, Yuchun Ma, Di Long, Xianlong Hong
EDA Lab, DCST of Tsinghua University
Beijing, China, 100084
*Email: dongsq@mail.tsinghua.edu.cn

Abstract –In the context of SOI, thermal constraint is more serious for analog devices. Besides the hot-spot effect, the temperature gradient on symmetrical devices may cause errors and even failures in the function. In order to handle these problems, this paper introduces an accurate thermal model into the placement process. Based on the geometric symmetry which is achieved with Corner Block List (CBL) for the first time, the thermal model helps to find the thermal-optimal placement. And the experimental results show this method is promising.

I Introduction

As the increase in frequency of the circuits and the widely use of SOI (silicon-on-insulator), thermal constraint is becoming more and more important, especially for analog devices, because these devices' operations rely greatly on the temperature. As power is dissipated in the channel of an analog device, the temperature rises due to the poor thermal conductivity of the relatively thick buried oxide layer of SOI. Then the risen temperature will affect the channel current through the carrier mobility, threshold voltage and velocity saturation mechanisms [1] and this may cause hot-spot and temperature gradient.

And the thermal constraint may be even more serious for symmetrical devices, for the symmetrical devices' operations rely more on the relative parameters of their corresponding devices than those of their own. However, the traditional works [2] [3] [4] [5] on symmetry constraint assume that the circuit is isothermal since the substrate material has good thermal conductivity. Therefore, they mainly focus on the geometric symmetry by using simulated annealing (SA) with some topological representations such as SP [2], TCG-S [3], segment tree [4] as well as Binary tree [5].

But this assumption must be questioned in the context of thermal-sensitive symmetrical analog devices and the use of SOI technology. The isolating buried oxide layer has a lower thermal conductivity, often over 100 times worse than silicon. As a result, even with the relatively moderate power levels encountered in typical signal path transistors, increases in the channel temperature of tens of degrees due to self-heating effect can be observed. And some of the heat generated by the distinct devices will flow laterally before reaching the substrate. Thus the devices around them will be affected, and the temperatures of these neighboring transistors will also rise. The temperature gradients resulting from self-heating and thermal coupling lead to nonisothermal conditions. This can lead to a much higher temperature on some devices and it is not consonant with the assumption for the traditional work on symmetry constraint.

The hot-spot effect may cause failure on the performance of analog devices, because high temperature will reduce drawn current dramatically. And the temperature gradients of symmetrical devices may cause mismatch or even failure on the performance. Therefore, it is very necessary to propose a method to handle thermal-driven symmetry constraint in order to decrease temperature gradients of symmetrical devices as well as to avoid hot-spot effect.

This paper introduces an accurate thermal model to evaluate the thermal condition of the analog layout with symmetry constraint which is achieved with CBL [6] representation for the first time. Decreasing the temperature gradients of symmetrical devices and avoiding hot-spot effect are both the thermal optimization objectives. The paper is organized as follows. Section II reviews the device-level thermal behavior and introduces the thermal model. Section III shows how to handle geometric symmetry constraint with CBL representation. Section Ⅳ gives the design and results of the experiments. Conclusions are drawn in Section Ⅴ.

II. Device-level Thermal Behavior and Thermal Model

A. Device-level thermal behavior

As described in the first section, the risen temperature of devices can affect the channel current through the carrier mobility, threshold voltage and velocity saturation mechanisms. The following three formulas [7] show the relations between the temperature and the three parameters above.

The carrier mobility decreases with the increase of temperature due to the increased scattering of electrons. And this effect is generally described by:

$$\mu_{eff} = \mu_{eff,0}(T/T_0)^{-k} \quad (1)$$

In (1), T_0 is the temperature of the environment and $\mu_{eff,0}$ is the effective mobility at T_0. And k is the mobility temperature exponent whose typical value is in the region of 1.5~1.7 for NMOS devices.

And the relation between threshold voltage V_T and temperature can be approximately expressed as:

$$V_T = V_{T0} - \lambda(T - T_0) \quad (2)$$

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In (2), V_{T0} is the threshold voltage at T_0 and λ is the threshold temperature coefficient with a typical value of -1~-3 mV/K for NMOS devices.

The critical field E_{SAT} is defined in the term of μ_{eff} and the carrier saturation velocity v_{SAT} which is also affected by temperature. An empirical formula is given as follows:

$$v_{SAT} = 2.4\times10^7 /(1+0.8\exp(T/600)) \quad (3)$$

The combination of these effects results in a reduction in drawn current with the increasing temperature. For single device, the too high temperature would lead to performance failure. And for the symmetrical/matching devices, the temperature gradient may cause mismatch or even failure on the performance. In [7], some experiments were carried out to test the relation between temperature and the performance of matching/symmetry devices. And the experimental results prove that the temperature gradient can affect the performance of matching/symmetry devices dramatically. And based on the analysis above, it is very necessary to take thermal effect into consideration during the placement process in order to guarantee the thermal-related performance.

B. Thermal model

The thermal model for calculating a placement of analog should consider both speed and accuracy, and then find a balance between them. Using simple models may overlook many potential problems such as the combined effect of different devices' heat dissipation within a certain area. And the model should not be too complex either, because the speed is also a very important factor for the placement algorithms.

In [8], an accurate thermal model which considers the combined effect of different heat dissipation modes is presented. Its assumption that the bottom of the substrate is insulated is very similar to the thermal effect based on the SOI technology in which the isolating buried oxide layer has a much lower thermal conductivity. Under this assumption, the overall heat escaping from the device can be visualized by Fig.1. The center of the device is the hottest point, and as the radius from the center increases, the heat decreases in monotonously in a Gaussian-like curve.

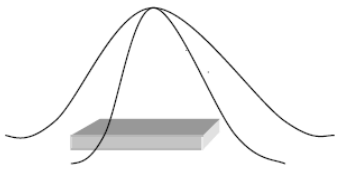


Fig.1 Thermal dissipation of a device

In order to denote the thermal effect more precisely, literature [8] uses radius coordinates. However, the analog devices are often seen as rectangles. Therefore, in this thermal model, a rectangular device with height *H* and width *W* is seen as a circle with the same area and the radius of the circle is $r=\sqrt{(W\times H)/\pi}$. And considering the SOI technology, $r=\sqrt{W\times(L+2L_H)/\pi}$ in which L_H is the thermal heating length [11].

This model assumes that the power density is a constant all over the chip. However, this assumption doesn't accord with the actual power distribution situation. Usually one device has its own distinct power density and its temperature usually scales up linearly with its power density. Therefore the device's power density is added into the thermal model for integrality.

Based on the analysis and assumption introduced above, the temperatures of the devices can be calculated with the following two equations.

$$T = P_d[c_1 I_0(md^+) + t^+/2B_i] \quad 0 \le d^+ < 1 \quad (4)$$

$$T = P_d c_4 K_0(md^+) \quad d \ge 1 \quad (5)$$

And the nomenclature of the two equations is as follows:

P_d: the power density;

T: the dimensionless temperature;

d: distance;

r: the radius of circle which denotes a rectangular device;

d^+: the dimensionless distance, d/r;

h: the convective heat transfer coefficient;

k: the thermal conductivity;

t: the thickness of the chip;

t^+: the dimensionless thickness, t/r;

$m=\sqrt{2h/kt}$;

B_i: the Biot number, ht/k;

$c_1=(-t^+/2B_i)/[I_0(m)+K_0(m)I_1(m)/K_1(m)]$;

$c4=-c_1 I_1(m)/K_1(m)$;

I_0, I_1 are the zeroth and first order modified Bessel functions of the first kind;

K_0, K_1 are the zeroth and first order modified Bessel functions of the second kind.

Note that the maximum temperature is in the center of the device, that is d =0. And because $I_0(0)$ =1, then equation (4) can be simplified as (6). The device's temperature can be represented by the maximum temperature.

$$T_{\max} = P_d[c_1 + t^+/2B_i] \quad (6)$$

According to (6), every device's temperature can be determined. And the thermal influence of every other device can be calculated by using (5). Then these values are summed to get the final result for the device being evaluated. And the combined thermal effect on each device can be expressed in (7). And Fig.2 visualizes this process.

$$T_i = T_{i0} + \sum_{j\neq i}^{M} T_{ji} \quad (7)$$

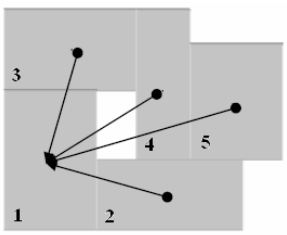


Fig. 2 Temperature evaluation of a device

III. Geometric symmetry on CBL representation

CBL [6] is composed of three sequences (S, L, T). Sequence S records the blocks' information from left-bottom corner to right-up corner. Sequence L records the direction of the modules' insertion operations, which "0" stands for vertical and "1" stands for horizontal. And Sequence T records the number of the T-junctions covered by every module in which "1" stands for a T-junction and "0" is the end symbol. Fig.3 shows an example of CBL, in which S is (*ABCDEFG*), L is (*100110*) and T is (*00101000*).

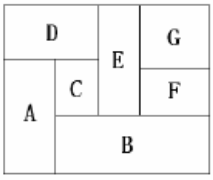


Fig.3 CBL representation

A. *Topological relation in CBL*

First, some symbols are introduced for formulation in which A and B stand for two modules.

S[A]<S[B], if A is before B in Sequence S.
S[A]>S[B], if A is after B in Sequence S.
A LT B, if A is to the left of B.
A RT B, if A is to the right of B.
A BW B, if A is below B.
A AE B, if A is above B.

In CBL, sequence L and sequence T describe the T-junctions' information covered by every module. Thus, it is difficult to use L and T to recognize the topological relations between modules. As a result of this, a tree structure called *T-bl*[10] which is show in Fig 4 in is created in order to handle this problem.

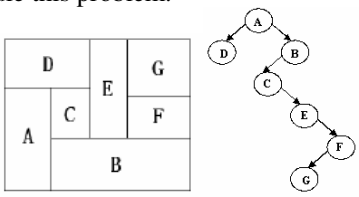


Fig.4 CBL and its T-bl

Lemma 1: Construction rules for T-bl
R(1) If two modules M and N are separated by a horizontal cutline, which share a common left boundary, and M is above N, M is N's left subtree.
R(2) If two modules M and N are separated by a vertical cutline, which share a common bottom boundary, and M is to the right of N, M is N's right subtree.
(Limited by the space, the proof process is omitted.)

Lemma 1 shows the rules for constructing T-bl. In Fig.4, A and D, B and C are constructed by *R(1)*. A and B, C and E are constructed by *R(2)*. And the construction process of *T-bl* can be finished in *O(n)* time in which *n* denotes the number of the modules.

In the data structure, every node in *T-bl* has its number labeled as *Treenum*. And the definition is that all the left subtree nodes' *Treenums* are less than that of their father node, while all the right subtree nodes' *Treenums* are more than that of their father node. Thus, every node's *Treenum* will be distinct. In Fig.4, D' *Treenum* is the minimum number, while F's is the maximal one.

With *Lemma 1*and the definition of *Treenum*, the topological relation between modules can be examined with the following theorem.

Theorem 1: Recognition of topological relations
If S[M]>S[N] and M' s Treenum<N's Treenum, M AE N.
If S[M]>S[N] and M' s Treenum>N's Treenum, M RT N.
(Limited by the space, the proof process is omitted.)

B. *Symmetry feasible CBL*

Compared with using *absolute* representations to handle symmetry constraint, the main advantage of using *topological* representations is that whether a random representation is symmetry-feasible or not can be affirmed before the packing process. And this can save a lot of time during the iterations of SA.

Therefore, how to handle this symmetry-feasible problem in CBL is the key to solve symmetry constraint with CBL. By examining the topological relations of modules in symmetry groups and self-symmetry modules, the conditions for feasible-CBL are proposed. In the following theorem, *M* and *M.sym* stand for the two modules which need to be placed symmetrically and for self-symmetry modules, *M = M.sym*. And we assume that all the k symmetry groups share a common vertical axis. (The horizontal axis can be handled similarly.)

Theorem 2: Conditions for Feasible-CBL
If all the k symmetry groups comply with the following two conditions, this CBL is a Feasible-CBL for symmetry.
C(1): For i=1 to k, Mi LT Mi.sym or Mi RT Mi.sym.
C(2): For i and j in [1,k] and i<>j,
If S[Mi]<S[Mj], S[Mi.sym]<S[Mj.sym] and Mi BW Mj, Mi.sym BW Mj.sym.
If S[Mi]<S[Mj], S[Mi.sym]>S[Mj.sym] and Mi LT Mj, Mi.sym RT Mj.sym.
(Limited by the space, the proof process is omitted.)

Take Fig.4 for example, (D, G) and (C, F) are symmetry groups and E is a self-symmetry module. D LT G and C LT F comply with *C(1)*. And S[D]<S[E], S[G]>S[E], D LT E LT G. Besides, (D, G) and (C, F) also accords with *C(2)*. And it is the same for (C, F) and E. Thus the CBL in Fig.4 is a feasible-CBL for symmetry constraint.

C. *Solution generator for symmetry-feasible*

According to *Theorem 2*, whether a CBL can be converted to placement with symmetry constraint can be examined. But it can't be used directly in simulated annealing to search for an optimal placement, because it has been proved by [2] that symmetry constraint would cause a great reduction to the feasible solution space. Therefore, it's necessary to propose a new solution generator to guarantee all the stochastic solutions are symmetry-feasible.

Based on T-bl, the original solution generator of CBL is modified to get the new one for symmetry-feasible.

Solution generator for symmetry-feasible:
(1) Exchange two modules in Sequence S. If the two modules belong to distinct symmetry groups, their symmetrical modules should also exchange their positions in T-bl;
(2) Exchange two modules' TreeNums. And similarly, if they belong to different symmetry groups, their symmetrical modules should also exchange their positions in Sequence S;
P.S. for (1) and (2), the swapping of a symmetrical module and a free module is invalid.
(3) Rotate modules. If the module belongs to a symmetry group, its symmetrical module should also be rotated.

And the requirement of multi-symmetry axes with the same orientation which is more general to analog circuit can be modeled in a similar way. First all the symmetry groups belonging to distinct axes should comply with *C(1)* and *C(2)* respectively. Then the new solution generation process should also comply with the solution generator for symmetry feasible. And this is also proved by the experimental results. (Fig.8)

IV. Experiment Design and Experimental Results

A. *Experiment design*

The objective of thermal-driven symmetry constraint is composed of three parts. The first one is high density of placement with symmetry, the second is decreasing temperature gradient on the two devices belonging to the same symmetry groups, and the last one is to avoid hot-spot effect.

High density can help to reduce delay but would cause high temperature according to the thermal model introduced before. However, the other two objectives can be improved with longer distance among devices. And further more, these two thermal objectives also depend on the relative positions of devices besides the distance factor. Equation (8) denotes the objective function for decreasing temperature gradient. And this equation reflects the average temperature difference of all the symmetry groups.

$$F_1 = \frac{1}{m}\sum_{i=1}^{m} | T_i - T_{i.sym} | \qquad (8)$$

In (8), m stands for the number of symmetry groups, not including self-symmetry devices, for self-symmetry devices don't have temperature gradient. T_i and $T_{i.sym}$ are the temperatures of the two devices in the same symmetry groups.

And equation (9) is the objective function for avoiding hot-spot. It is achieved by decreasing the difference of T_j and T_{avg}.

$$F_2 = \sum_{j=1}^{n} (|1 - \frac{T_j}{T_{avg}}|) \qquad (9)$$

According to (8) and (9), the whole objective function (10) that is used in simulated annealing is proposed, in which w_1, w_2 and w_3 are weight coefficients. In order to guarantee the performance, w_2 and w_3 will be considered first.

$$F = w_1 \times Area + w_2 \times F_1 + w_3 \times F_2 \qquad (10)$$

Equation (10) shows that this is a multi-objectives optimization process. Though SA can find a tradeoff among the different objectives, one heuristic strategy is also adopted to enhance the quality of solution.

Because different devices have different power density and area, then they have different "thermal-effect" ability. With stronger "thermal-effect" ability, the device can influence others' temperatures more dramatically. And if t is a constant, (5) can be converted to the following equation.

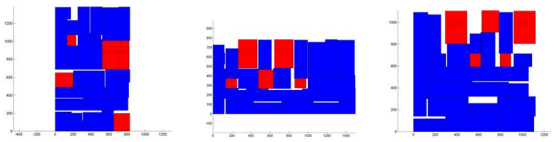
$$T = \frac{P_d}{r} \times Cons \times K_0(md^+) \quad d \geq 1 \qquad (11)$$

In (11), *Cons* denotes the constant part and $K_0(md^+)$ denotes the distance effect. Therefore, the "thermal-effect" ability of a device is determined by P_d/r which *TEA* is used to denote it. Then every device's *TEA* can be calculated and the device with the maximum *TEA* is chosen as the self-symmetrical device. Because self-symmetrical devices affect the temperatures of the devices in one symmetry group equally, this strategy can help us to decrease the temperature gradient between symmetrical devices.

B. *Experimental results*

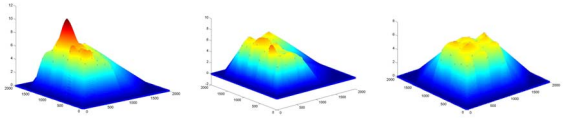
First the algorithm is first tested on the MCNC benchmarks. Some modules are selected and modified randomly to be the symmetrical devices. And the experimental results under three different conditions are compared: (a) without symmetry constraint, (b) only with symmetry constraint, (c) with both symmetry and thermal constraints. Table I shows the results. From this table, it is clear that symmetry can help to reduce temperature gradient, while our algorithm can almost eliminate temperature gradient and avoid hot-spot.

Fig.5, Fig.6 and Fig.7 show the placement and heat distribution for ami33. In Fig.5, the self-symmetrical module is the one with the maximum *TEA*. In Fig.6, the warmer color denotes the higher temperature. And in Fig.7, the numbers like 1,2,3 in the figure denote the positions of the symmetrical devices. The devices belonging to the same symmetry group almost locate on the same isotherm.



(a) (b) (c)

Fig.5 (a) Without constraint; (b) With symmetry; (c) With both symmetry and thermal constraints



(a) (b) (c)

Fig.6 (a) Without constraint; (b) With symmetry; (c) With both symmetry and thermal constraints

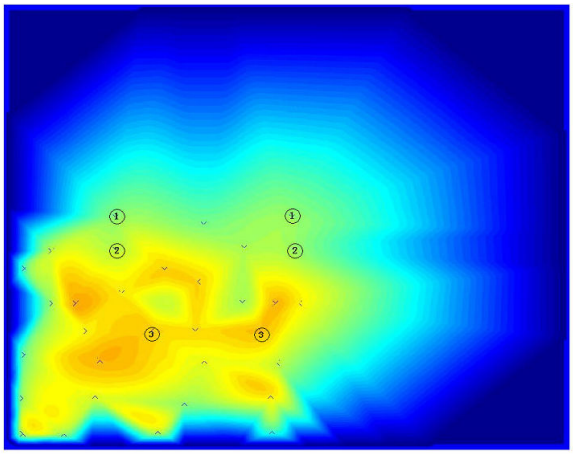


Fig.7 the planform of heat distribution

This method is also tested on a case with several distinct symmetry axes which have the same orientation. In Fig.8, there are three distinct symmetry axes. And its T_{max} is 9.5 and F_1 is 1.4%.

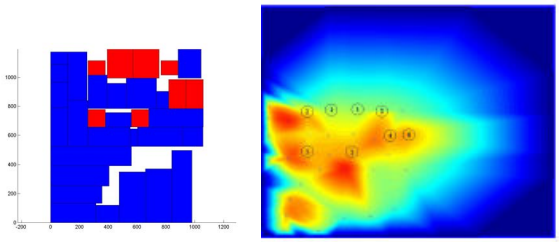


Fig.8 (a) Placement and of multi-symmetry axes
(b) Heat distribution of multi-symmetry axes

At last, an actual analog circuit is also been tested. Fig.9 shows the schematic of the circuit in which (M1a, M1b), (M2a, M2b), (M3a, M3b), (M4a, M4b) are symmetry groups generated by [9]. And M5 is a self-symmetry device. The final layouts and heat distribution results under two conditions: (a) only with symmetry constraint, (b) with both symmetry and thermal constraints are also proposed in Fig.10, Fig.11 and Fig.12.

In Fig.10 (b), M10 is the device which is with maximum *TEA*. And Fig.10 shows that our algorithm is effective for avoiding hot-spot. The heat is distributed more averagely on the whole substrate. The planforms of the heat distribution are shown in Fig.12. And the numerical results are given in Table Ⅱ .

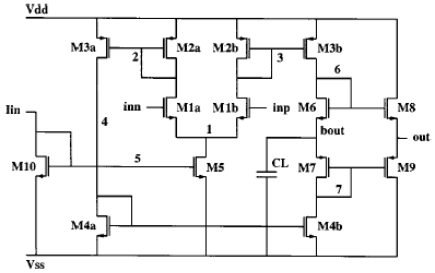


Fig.9 Schematic of a high-speed CMOS comparator

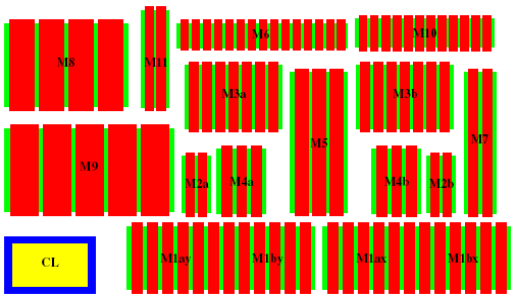


Fig.10 (a) Layout with only symmetry constraint

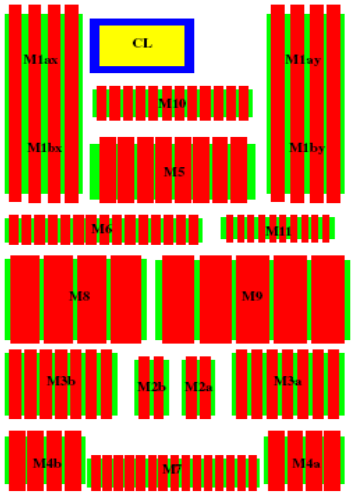
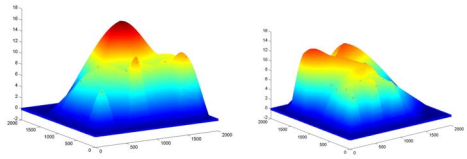


Fig.10 (b) Layout with both symmetry and thermal constraints



(a) (b)

Fig.11 (a) Only with symmetry constraint;
(b) With both symmetry and thermal constraints

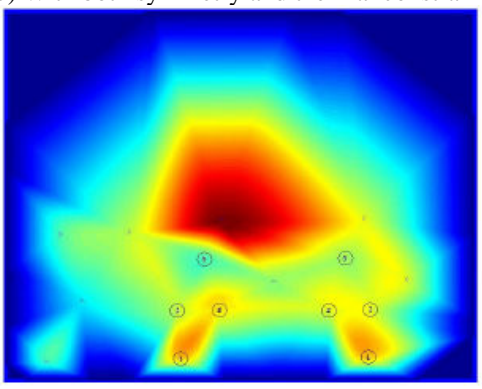


Fig.12 (a) Heat distribution planform with only symmetry

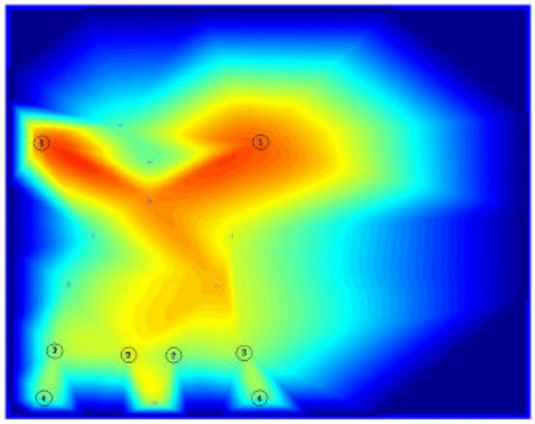


Fig.12 (b) Heat distribution planform with both symmetry and thermal constraints

Table Ⅱ Results for high-speed CMOS comparator

	No. of devices/ Symmetry groups	T_{avg}	T_{max}	F_1	Time(s)
Only with symmetry constraint	16/4	9.81	17.19	7.8%	37.9
With both symmetry and thermal constraints	16/4	9.77	13.21	3.5%	100.7

V. Conclusions

According to the analysis of thermal influence on matching/symmetry devices in analog circuit, it is clear that too high temperature on single device would cause performance failure and temperature gradient can affect the performance of symmetrical devices dramatically. Therefore, based on the traditional geometric symmetry constraint which is achieved with CBL representation for the first time, a thermal model is introduced to the placement process in order to decrease temperature gradient and avoid hot-spot. The final experimental results prove the effectiveness of our algorithm.

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Table Ⅰ Experimental results on MCNC benchmarks

Circuit	Module numbers/ Symmetry groups	Without constraint				Only with symmetry constraint				With both symmetry and thermal constraints			
		Area usage	T_{avg}	T_{max}	F_1	Area usage	T_{avg}	T_{max}	F_1	Area usage	T_{avg}	T_{max}	F_1
ami33	33/3	94.6%	6.9	11.5	14.3%	93.1%	6.87	8.25	5.2%	87.9%	6.88	7.88	2.7%
ami49	49/3	91.4%	11.2	17.6	17.2%	85.8%	11.1	14.3	11.9%	83.3%	10.9	11.4	3.17%
Hp	11/2	95.9%	8.58	14.52	28.3%	92.9%	8.49	12.64	14.5%	90.9%	8.62	10.64	7.25%
Apte	8/3	97.9%	5.67	10.43	35.1%	98.4%	5.67	10.42	11.5%	97.5%	5.59	9.82	6.7%
xerox	10/3	95.9%	5.51	8.91	20.9%	95.7%	5.43	7.34	7.8%	93.9%	5.48	7.22	2.5%