A new test and characterization scheme for 10+ GHz Low Jitter Wide Band PLL

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Abstract - This paper presents a new test and characterization scheme for 10+ GHz low jitter wide band PLL in 90 nm partially depleted (PD) Silicon-On-Insulator (SOI) CMOS technology. We measure the frequency range of VCOs without adding any devices for test between charge-pump (CP) and voltage- controlled oscillator (VCO). That test scheme gives us the intermediate frequency of VCO as well as the maximum and the minimum frequency. This paper also describes circuitry to observe the duty cycle of 4.2GHz clock directly on a wafer probe station, including a method to verify the measured duty cycle.

I. Introduction

A high performance microprocessor with multigigahertz operating frequencies becomes more ubiquitous than before since even consumer appliances like game consoles or low-end servers recently require it in addition to personal computers and high-end servers. In order to generate a very high frequency system clock, the microprocessor must implement phase locked loops (PLL's), the performance of which reach 10+ GHz operating frequency in some cases [1].

As a frequency of PLL becomes higher, the PLL should have more superior characteristics like a lower jitter, a higher and wider frequency range of VCO, and a well-controlled duty cycle of an output clock. It, however, is very hard to test or measure those characteristics, especially more difficult on manufacturing because a tester has a restricted specification mainly.

Some good schemes to characterize a high performance PLL are already proposed, and they try to add some devices or circuits in order to make the PLL open-loop in measurement. Those appendages, however, may negatively affect the characteristics of PLL themselves; for instance, induced noise from additional devices on an input node of voltage-controlled oscillator (VCO) gets a jitter of PLL high, or an adding multiplex circuit at an output of PLL makes the duty cycle of that output vary. We have a lot of interests in the scheme to characterize a high performance PLL without giving it negative influence, and that scheme should be able to use on manufacturing in order to screen the PLL. A frequency range of VCO should be focused on since it is one of the most important parameters to determine the characteristics of PLL.

It is generally desirable for a duty cycle of a system clock bring it close to 50% as much as possible. A high performance microprocessor, however, has a situation demanding the duty cycle that is not 50% precisely since it uses both the edges of a system clock though it is not a DDR (Double Data Rate) system. One of the greatest concerns about the duty cycle of the high frequency system clock is to know what duty cycle is optimum for the microprocessor or the circuit. We propose circuitry to observe the actual duty cycle of the high frequency clock directly.

The proposed scheme uses unique circuits and I/Os for observing divided clocks and a duty cycle of the clock has easily varied just by going through a simple circuit like an inverter. So we try to verify the duty cycle that is measured by that scheme.

II. How to characterize PLL

A. A frequency range of VCO

A simplified block diagram of the PLL architecture with VCO test mode is shown in Fig. 1, the power of which is supplied by analog vdd (VDDA). Outputs of a phase-frequency detector (PFD), “UP1B” and “DN1”, are directly fixed to VDDA or analog gnd (GNDA) by control signals, “UP_ctrl”, “DN_ctrl”, “VCO_test” and “VCO_ini” instead of implementing additional devices between charge-pump (CP) and VCO in order to apply some voltages to “CTRL” node.

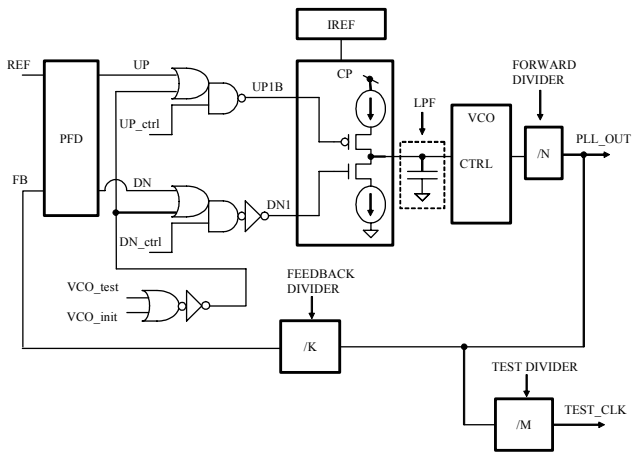

Fig. 1. Simplified PLL architecture with VCO test mode.

In a normal operation mode, both UP_ctrl and DN_ctrl are set to high level (“H”), and both VCO_test and VCO_ini are set to low level (“L”). When VCO_ini is asserted and UP_ctrl is set to “L” in the normal operation mode, CP is in state of discharge then the frequency of VCO becomes the minimum eventually. This function is used during power on reset (POR) sequence in order to initialize the PLL.

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As VCO_test is asserted, the PLL gets into VCO test mode. By setting UP_ctrl to “L” and DN_ctrl to “H”, the frequency of VCO becomes the minimum like PLL initialization mode mentioned above. “PLL_OUT” goes to not only a tree of clock distribution but also another divider for PLL characterization, and the divided clock is observed out of a chip. By setting UP_ctrl to “H” and DN_ctrl to “L”, CP is in state of charge then the maximum frequency of VCO is measured. When both UP_ctrl and DN_ctrl are set to “H”, CP makes crowbar current and outputs intermediate voltage at “CTRL” node. It means that the intermediate frequency of VCO is observed.

B. Duty cycle of PLL output

Since PLL power is supplied by VDDA and the logic circuits that work with the PLL output are powered by digital vdd (VDD), PLL-to-logic level shifters are necessary between the PLL and the logic circuits. The level shifter (LS), however, may make duty cycle variation, so we have to make great attention to design it and try to measure the duty cycle of the LS output.

Fig. 2 and Fig. 3 show a simplified block diagram of a duty cycle measurement apparatus and a logic waveform of it respectively. There are two identical counters with clear mode in that apparatus, one operates with “CLK” and the other does with “/CLK”. Outputs of those counters, “N18” and “N28”, have a same period (16 times of CLK period), and the phase difference between N18 and N28 is the same time period as the pulse width of CLK. In other words, a pulse width of a very high frequency clock is taken out as a phase difference between two lower frequency clocks that can be more easily observed. It, however, is not easy to measure a phase difference between two clocks precisely on a basic digital oscilloscope. So “OUT160” and “OUT155” are prepared to measure the pulse width of CLK actually. OUT160 has the same pulse width as N18, while OUT155 has a short pulse width than N28 for the pulse width of CLK. It is easier to measure a pulse width of a clock on a basic digital oscilloscope and a difference of pulse width between OUT160 and OUT155 is the same time period as the pulse width of CLK. By using this scheme, a very short time period like 125ps (equivalent pulse width of 4GHz clock) can be observed on even a wafer probe station, the pass bandwidth of which is lower than 1GHz generally.

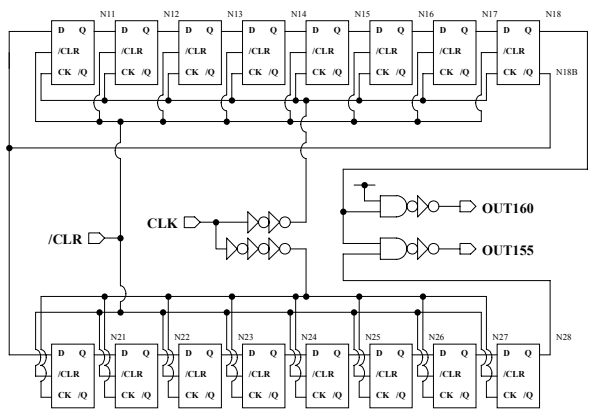

Fig. 2. Simplified duty cycle measurement apparatus.

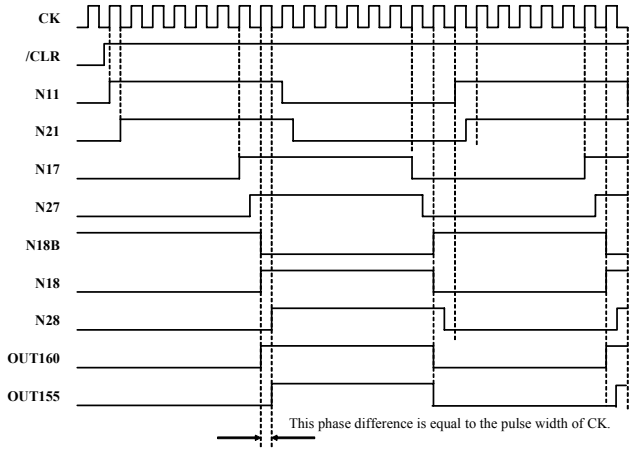

Fig. 3. Logic waveforms of duty cycle measurement apparatus.

C. Verification method of measured duty cycle

The duty cycle measurement apparatus described in the preceding paragraph is implemented in order to observe the duty cycle variation that is made by LS. We try to take out the duty cycle of the clock correct as possible; for instance making the parasitic resistance and capacitance on the clock path of OUT160 and one of OUT155 the same, maintaining the identity of two counters, and so on. The results, however, may not be correct because of an unexpected factor. So another circuitry to verify a measured duty cycle of the clock is also implemented.

Simplified duty cycle verification circuitry is shown in Fig. 4, which contains 4+ GHz PLL, three candidates of LS and the duty cycle measurement apparatus, too. First candidate of LS is a simple inverter, the output of which is “CK1”. Second one is an AC-coupled type, the output of which is “CK2”, and last one is an inverter with duty cycle adjuster (DCA), which can change a duty cycle of the output by applying analog voltage (Vbias0). The output of last one is “CK3”. One of three clocks is selected at MUX1 that can also invert the input clock.

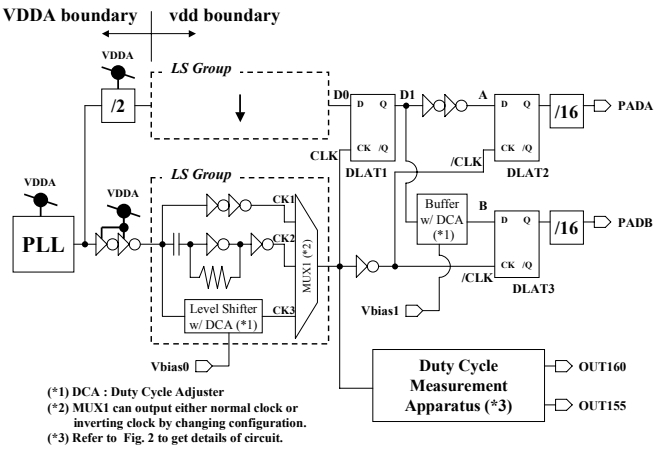

Fig. 4. Simplified duty cycle measurement and verification circuitry.

"D0" is a divided clock by two and a data signal for D-latch (DLAT1). "D1" is a latched clock by CLK that is an output clock of MUX1. "A" is just a buffered clock and a data signal for another D-latch (DLAT2), while "B" is a buffered clock changing duty cycle of "D1" by applying another analog voltage (Vbias1) and a data signal for DLAT3. As Vbias1 is lower, the pulse width of B is narrower. When Vbias1 is swept, latching the data (B) begins to fail at certain voltage, which is defined as V_{fail}. Since B is latched by "/CLK", V_{fail} is related to the duty cycle of CLK.

Fig. 5 shows logic waveforms of duty cycle verification circuitry in Fig. 4. CLK' describes a clock that has a smaller duty cycle than 50%. When /CLK', which is the inverted clock of CLK', is input to "CK" of DLAT3, V_{fail} (=VH) is higher than the voltage (V_{fail}=V50) which latching the data (B) begins to fail at in the case of 50% duty cycle. In contrast CLK'' describes a clock that has bigger duty cycle than 50% and V_{fail} (=VL) is lower than V50. If the duty cycle of CLK is around 50%, VH is very close to VL at least. Expressed in another way, as the voltage difference between VH and VL is big, the duty cycle of CLK is off 50%.

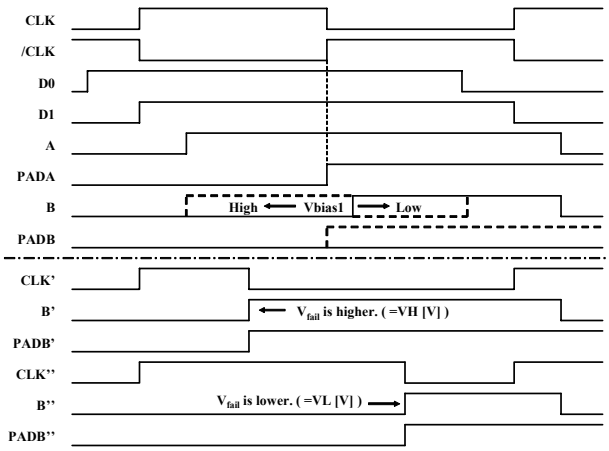

Fig. 5. Logic waveforms of duty cycle verification circuit.

III. Experimental Results

Both a tracking range of 10+ GHz low jitter wide band PLL and a frequency range of VCO implemented in that PLL were characterized on the actual products using the customized module test station with custom pattern generator hardware. In contrast, the duty cycle of the PLL output was tested on unpackaged PLL testsite die using a Cascade Microtech Summit probe station, 25 pad GGB Industries multi-contact wedge probes with integral bypass capacitors and coax cables, and assorted power supplies. Agilent 8133A pulse generator and 54855A sampling scope, and custom pattern generator hardware were used in all measurements.

A. Compare a frequency range of VCO with a tracking range of PLL

Fig. 6 provides the tracking range of 10+ GHz low jitter wide band PLL and the frequency range of the VCO versus the power supply voltage of the PLL (VDDA). The range between "Tracking_Low" and "Tracking_High" is the tracking range of the PLL, and the range between "VCO_Min" and "VCO_Max" is the frequency range of the VCO that was measured by using VCO test mode. Here are the dividing ratios in the measurement; the dividing ratio (=N) of FORWARD DIVIDER in Fig.1 is 2, the dividing ratio (= K) of FEEDBACK DIVIDER is 8, and the dividing ratio (=M) of TEST DIVIDER is 8. A clock more than 1GHz was input as a reference clock in order to measure the maximum tracking frequency in this condition.

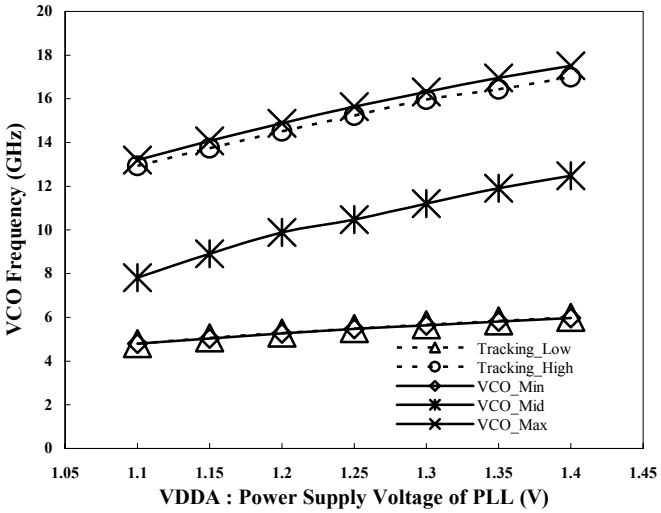

Fig. 6. Tracking range of PLL and frequency range of VCO versus power supply voltage of PLL.

A tracking range is one of most important parameters to know an actual performance and characteristics of PLL or to screen PLL. It, however, takes a long time to measure it generally since it is necessary to sweep a reference clock ("REF" in Fig. 1) and to change a power supply voltage of PLL every measurement. It, furthermore, is difficult to input a very high frequency clock more than 500MHz into REF on manufacturing because of the restriction that a basic tester has a lower bandwidth of the input.

Measuring the frequency range of the VCO by using VCO test mode on manufacturing is much easier than measuring the tracking range since VCO test mode does not require any clocks as an input. According to Fig. 6, the tracking range of the PLL is almost the same as the frequency range of the VCO, and the ratio between VCO maximum and minimum frequency was very close to the design value, 2.7 to 2.9. It means that the VCO test mode can be used in order to screen the PLL on manufacturing. This is very useful for reducing test time.

B. Actual duty cycle of a 4.2GHz clock

Fig. 7 shows an oscilloscope view in which the waveforms of the low frequency clocks, which is OUT160 and OUT155 in Fig. 4, were observed in order to measure the pulse width of the very high frequency clock, which is CLK in Fig. 4. The difference between rising edges of two clocks (265MHz) is equal to pulse width of a 4.2GHz clock, the actual time period is 104.8ps and the duty cycle is 44%.

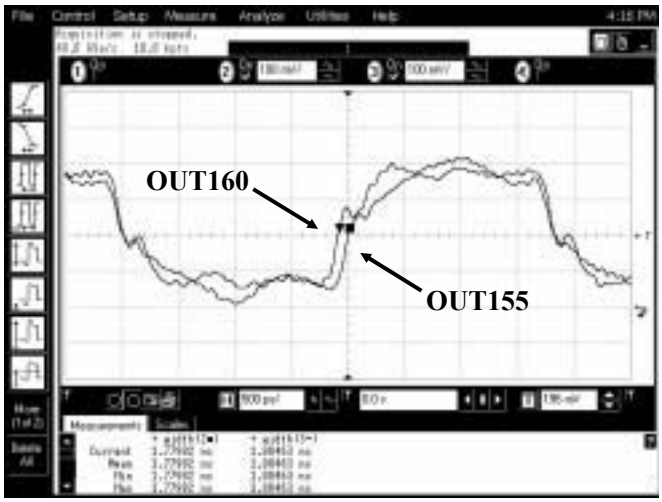

Fig. 7. An oscilloscope view of the pulse width measured for 4.2 GHz clock. The difference between rising edges of two clocks is equal to the pulse width of 4.2GHz clock.

Fig. 8 provides the actual duty cycle of the 4.2GHz clocks, which are CK1, CK2 and CK3 in Fig. 4, versus a voltage difference between VDDA and VDD. We try to describe the duty cycle variation that is made at LS in Fig. 4 in relation to the voltage difference in addition to the actual duty cycle in that chart. The duty cycle of CK2 must be the same as the output of the PLL in Fig. 4 because AC-coupled LS transfers a duty cycle of the input to the output precisely. It means that the output of the PLL in this testsite die seems to have roughly 10% offset of duty cycle originally since the output of VCO is divided by two at FORWARD DIVIDER and the duty cycle of the PLL output must be close to 50%. In addition, LS with DCA can correct that offset and the duty cycle variation at AC-coupled LS has no dependency on the difference between two power supply voltages. This shows a right result according to AC-coupled LS characteristics.

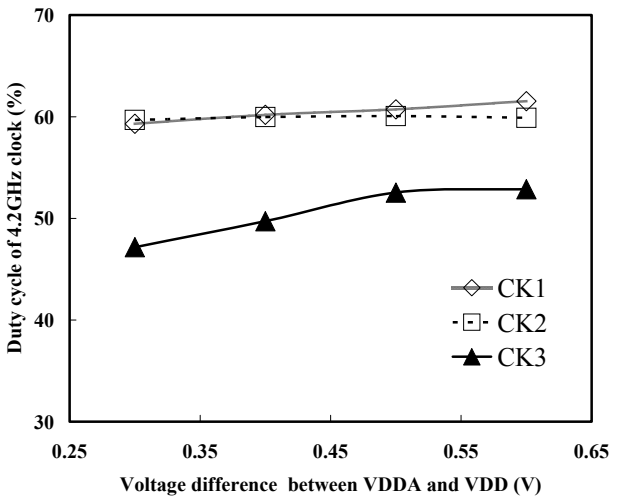

Fig. 8. The duty cycle of 4.2GHz clocks versus a difference between two power supply voltages. CK1, CK2 and CK3 are outputs from different type of level shifters.

We strongly believe that all of the relative information is right in Fig. 8, and it is necessary to verify the actual value of duty cycle as the next step.

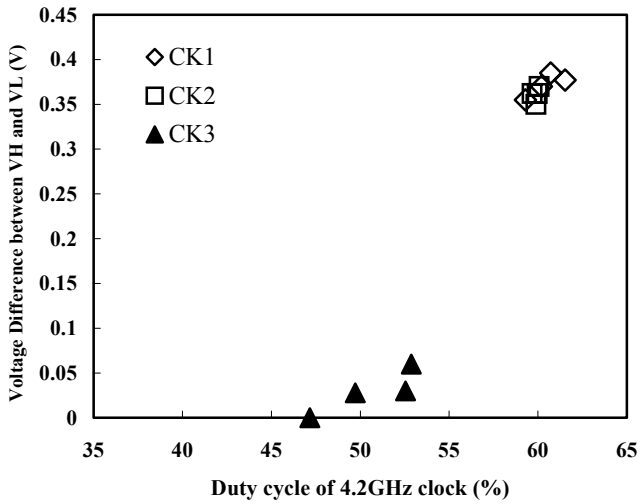

Fig. 9. The duty cycle of 4.2GHz clock versus a voltage difference between VH and VL that are applied biases for DCA. VH is V_{fail} in the case of using a normal clock, and VL is V_{fail} in the case of using the clock inverting the normal clock.

Fig. 9 provides the duty cycle of 4.2GHz clock versus a difference between two voltages of V_{fail}. At this point, VH is the measured voltage in the case of using certain CLK (=Clk_A) and VL is the measured voltage in the case of using the clock that is made by inverting Clk_A. If the duty cycle of CLK is around 50%, the voltage difference between VH and VL is close to 0V. It means that the duty cycle of CK3 must be around 50%, and it agrees with the duty cycle in Fig. 8. On the other hand, the voltage difference between VH and VL in the case of CK1 or CK2 is higher than 0.35V. A big voltage difference means that the duty cycle of the clock is off 50%, and in fact the duty cycle of CK1 or CK2 is around 60% in Fig. 8. As a result, the duty cycle that is measured by the new scheme in Fig. 2 is verified by another new scheme in Fig. 4.

IV. Summary and Conclusions

We have reported a new test and characterization scheme for a high performance PLL. By using VCO test mode, a frequency range of the VCO can be easily measured without jitter penalty on even manufacturing test and a tracking range of the PLL will be able to be predicted from that measurement result. The duty cycle measurement apparatus is suitable for characterizing a high performance PLL or a system clock of a microprocessor with multigigahertz operating frequencies under a general test environment, which needs lower setup cost. We also verified the accuracy of measured duty cycle at 4+ GHz.

References

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