Parallel-Distributed Time-Domain Circuit Simulation of Power Distribution Networks with Frequency-Dependent Parameters

Takayuki WATANABE

School of Administration and Informatics,
University of Shizuoka,
52-1, Yada, Suruga-ku, Shizuoka,
422-8526,Japan.
Tel/Fax: +81-54-264-5433
e-mail: watanat@u-shizuoka-ken.ac.jp

Yuichi TANJI

Dept. of Reliability-based Information Systems Engineering, Faculty of Engineering, Kagawa University,
2217-20, Hayashi, Takamatsu,
761-0396, Japan.
Tel/Fax: +81-87-864-2235/2262
e-mail: tanji@eng.kagawa-u.ac.jp

Hidemasa KUBOTA Hideki ASAI

Department of Systems Engineering,
Faculty of Engineering,
Shizuoka University
3-5-1, Johoku, Hamamatsu,
432-8561, Japan
Tel/Fax: +81-53-478-1237/1269
e-mail: hideasai@sys.eng.shizuoka.ac.jp

Abstract - In this paper, we focus on the verification of the PCB/Package power integrity, which becomes very important for the design of state-of-art high speed digital circuits. The simulation of power distribution networks (PDNs) of the PCB/Package, which can be modeled as a large number of RLC lumped components, is a time-consuming task for using the conventional circuit simulator, such as SPICE. For this problem, we propose a parallel-distributed time-domain circuit simulation algorithm based on LIM. Furthermore, an effective modeling of frequency-dependencies of the PDNs, such as skin effects and dielectric losses, to solve by LIM is proposed.

I. Introduction

In the design of high-speed digital circuits, it is important to model the power distribution networks (PDNs) of the PCB/Package in order to estimate and analyze unwanted noises, such as ground bounce, delta-I noise, and simultaneous switching noise (SSN). Usually, the PDNs of the PCB/Package are designed using multilayered power/ground plane pairs. Due to the transient switching current of the CMOS transistors, voltage fluctuations are generated by the parasitic inductances/capacitances of the planes, and the power plane resonance causes a performance degradation of the system. Then, taking measures in the early stages of design enables improvement of quality and reduction of cost [1].

Detailed analysis of the PDN using full-wave electromagnetic simulators provides accurate results. However it takes enormous CPU time and huge memory capacity. In the case of on-chip power distribution grids, the PDN can be modeled as power and ground (P/G) lines. On the other hand, in the case of the PCB/Package, the PDN can be modeled as two-dimensional P/G planes in many cases. As is well known, each P/G plane pair can be discretized spatially into (M−1) × (N−1) unit cells as shown in Fig. 1 [2]. Each RLGC parameter of the equivalent circuit of the unit cell is derived by dimensions and medium coefficients. Therefore, instead of full-wave simulators, if the power plane is modeled as a large number of lumped RLC components, the conventional circuit simulator, such as SPICE, is available. However, it is still difficult to analyze them using SPICE, because of the large scale of the PDN circuit.

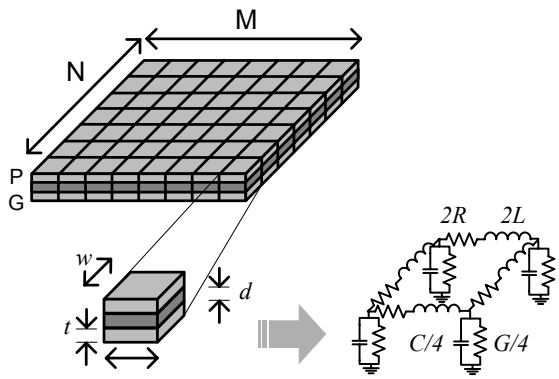

Fig. 1. Unit cell and equivalent circuit of PDNs.

For these problems, Latency Insertion Method (LIM), which is an algorithm for the time-domain simulation of large networks, is effective [3][4]. LIM is the derivative method in a class of the algorithms such as "leapfrog" finite-difference time-domain (FDTD) method [5][6]. Hence, LIM is sometimes referred to as the “circuit-based FDTD” method. That is to say, the node voltage vector and the branch-current vector are computed alternately. It can analyze large RLC networks very efficiently with much lower calculation cost of solving simultaneous equations in contrast to the implicit numerical integration used in SPICE-like simulator.

Because LIM is based on the basic leapfrog time stepping scheme, several parallel computation techniques can be applied to it [7]. Using these techniques, the whole circuit to be analyzed is divided into several subcircuits, and each subcircuit is simulated by each PE (Processing Element). In this paper, a parallel-distributed LIM algorithm is proposed to achieve a faster time-domain simulation of larger scale PDNs.

Also, actual PDNs have some frequency-dependent properties, such as skin effects and dielectric losses. In [8], high-speed interconnects having these frequency-dependent parameters were represented as the lumped segmentation model. Each segment can be obtained from the Debye rational function which approximates the frequency-dependent parameters. This segmentation model was solved by an LIM-like leapfrog time stepping scheme. However, this scheme has a limitation of the circuit structure

0-7803-9451-8/06/$20.00

to be analyzed. That is to say, every branch must have an inductor and every node must be connected with the grounded capacitor [9]. Because the model of [8] does not meet these conditions, every first-order Debye model of each segment had to be solved via matrix inversion in order to apply LIM to solve the whole interconnect model. In this paper, we propose an effective modeling of frequency-dependent parameters for LIM simulation. In our modeling, the circuit representation of the first-order Debye function is modified to a suitable form for LIM. Finally, some PDN examples are simulated and the efficiency of our method is verified.

II. Latency Insertion Method

In this section, we briefly introduce LIM [3][4]. The circuit to be analyzed by LIM requires that each branch has an inductor and each node has a grounded capacitor as shown in Fig. 2. For the branch which consists of a series of an inductor, a resistor and a voltage source as shown in Fig. 3(a), the KVL equation is obtained by

$$V_i^{n+1/2} - V_j^{n+1/2} = L_{ij}\left(\frac{I_{ij}^{n+1} - I_{ij}^{n}}{\Delta t}\right) + R_{ij} I_{ij}^{n} - E_{ij}^{n+1/2} \quad (1)$$

Then, the branch current is updated, as in

$$I_{ij}^{n+1} = I_{ij}^{n} + \frac{\Delta t}{L_{ij}}\left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^{n} + E_{ij}^{n+1/2}\right), \quad (2)$$

Each node has a parallel combination of a capacitor, a conductance and a current source to the ground as shown in Fig. 3(b). Then, KCL leads to

$$C_i\left(\frac{V_i^{n+1/2} - V_i^{n-1/2}}{\Delta t}\right) + G_i V_i^{n+1/2} - H_i^{n} = -\sum_{k=1}^{M_i} I_{ik}^{n}, \quad (3)$$

where M_i is the number of branches connected to the node. Then, the node voltage is updated as

$$V_i^{n+1/2} = \frac{\frac{C_i}{\Delta t} V_i^{n-1/2} + H_i^{n} - \sum_{k=1}^{M_i} I_{ik}^{n}}{\frac{C_i}{\Delta t} + G_i}. \quad (4)$$

Time-domain simulation is done by the alternate "leapfrog" updates of branch-currents and node-voltages according to (2) and (4). To simulate stably, the time step Δt is determined based on the minimum values of inductance and capacitance in the circuit as follows,

$$\Delta t \le \sqrt{LC}. \quad (5)$$

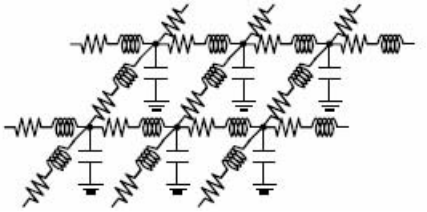

Fig. 2. Circuit structure suitable to LIM.

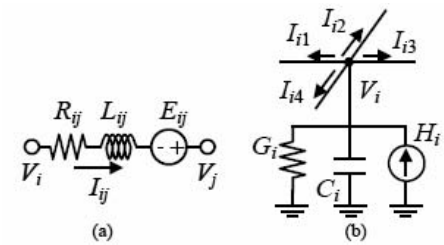

Fig. 3. Branch and node in LIM. (a): branch. (b): node.

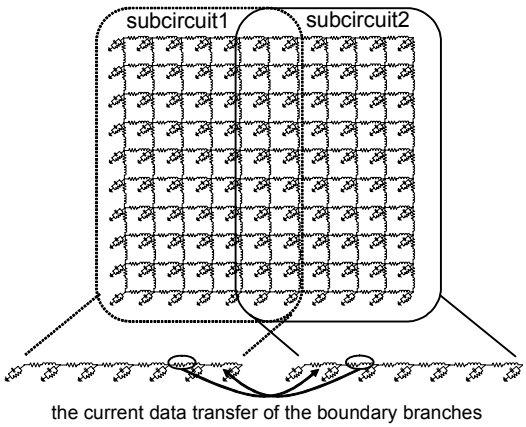

Fig. 4. Partitioning the PDN circuit.

III. Parallel-Distributed LIM Algorithm

Because LIM is based on the basic leapfrog time stepping scheme, it is faster than the conventional circuit simulator such as SPICE which requires solving the large sparse system of equations. However, there is still a limit to the size of the circuit which can be solved by one PE (Processing Element) even in LIM. To address this problem, the parallel-distributed LIM algorithm is proposed in this section. Actually, we have already developed the parallel-distributed full-wave FDTD simulator [7]. Because of similarities between LIM and full-wave FDTD, several parallel computation techniques of full-wave FDTD could be applied to LIM.

First of all, our algorithm divides the whole circuit into some subcircuits, and each subcircuit is assigned to different computer resource and analyzed by each PE on a PC-cluster. In the case of a planer power/ground structure, it is easy to divide the circuit into subcircuits as illustrated in Fig. 4.

Next, for calculating voltage of a node located at the boundary part of each subcircuit, the past values of the

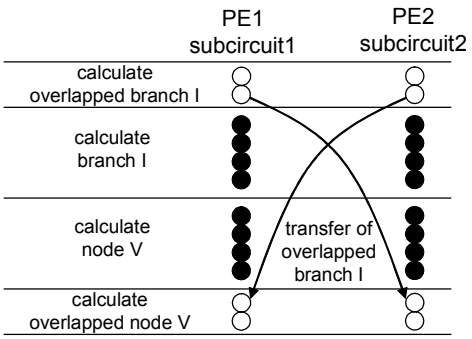

Fig. 5. Parallel-distributed LIM algorithm

branch current on the neighboring subcircuit, namely, on the adjoining PC, is required in each time step. Therefore, each subcircuit is chosen so that the boundary nodes overlap as illustrated in Fig. 4. While the communication speed between computers is usually slower as compared with the speed of the memory transfer in a computer, the time required for a current data transfer of the boundary branches can be ignored because the number of boundary nodes is relatively small, and the data transfer of the boundary branches and the calculation of node voltages and branch currents except the boundary can execute simultaneously. Finally, our algorithm is summarized in Fig. 5.

IV. Frequency-Dependent Parameters

A. first-order Debye model

In this section, we discuss the modeling of frequency-dependent parameters of PDNs. Actual PDNs have some frequency-dependent properties, such as skin effects and dielectric losses. These properties can not be simulated by the frequency-independent unit cell as illustrated in Fig. 6(a). Instead of this model, in order to simulate frequency-dependent effects, we can use the frequency-dependent transmission line model, such as the W-element of the Synopsys's Star-Hspice as illustrated in Fig. 6(b) [2]. In this case, the distributed series impedance and shunt admittance of the transmission line are defined as

$$Z(\omega) = R_{dc} + j\omega L_{ext} + R_{ac}\sqrt{\omega}(1+j), \tag{6}$$

$$Y(\omega) = G_{dc} + \omega G_d + j\omega C, \tag{7}$$

where

$$R_{dc} = \frac{2}{\sigma_c t}, \quad R_{ac} = \sqrt{\frac{2\mu_0}{\sigma_c}},$$
$$L_{ext} = \mu_0 d, \tag{8}$$
$$G_d = \varepsilon_0 \varepsilon_r \frac{w^2}{d} \tan(\delta),$$

where σ_c is the conductivity of the conductor, μ is the permeability, ε is the electrical permittivity, $\tan(\delta)$ is a loss tangent of the material. Also w, t and d are defined in Fig. 1. As a result, frequency-dependent RLGC parameters of PDNs are analytically obtained as following forms:

$$R = R_{dc} + R_{ac}\sqrt{\omega},$$
$$L = L_{ext} + \frac{R_{ac}}{\sqrt{\omega}},$$
$$G = G_{dc} + \omega G_d, \tag{9}$$
$$C = \varepsilon_0 \varepsilon_r \frac{w^2}{d}.$$

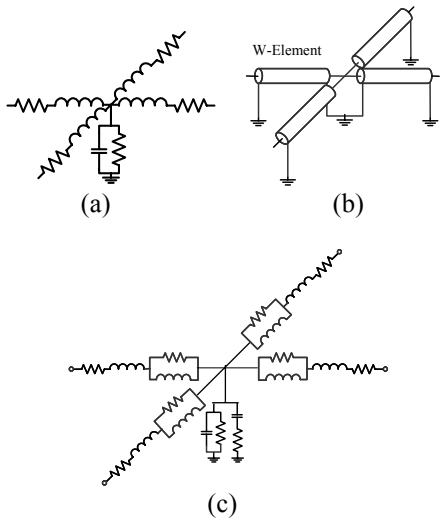

Fig. 6. Several types of unit cell model.
(a): frequency-independent model. (b): W-element model. (c): first-order Debye model.

```
.SUBCKT RL2 p1 p2
R0  p1 2   1.149426e-003
L0  2  3   2.514000e-010
R1  3  4   1.350000e-006
L1  3  4   6.750000e-008
R2  4  5   1.450000e-005
L2  4  5   1.611111e-008
R3  5  6   7.616400e-003
L3  5  6   1.904100e-011
R4  6  p2  3.188935e-002
L4  6  p2  3.188935e-012
.ENDS
```

```
.SUBCKT GC4 p1 p2
C0   p1  p2  1.245094e-012
RG1 p1   2   1.453488e+004
C1   2   p2  8.600000e-014
RG2 p1   3   6.806425e+002
C2   3   p2  4.897333e-014
.ENDS
```

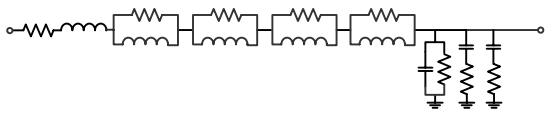

Fig. 7. a concrete example of the Debye model.

Usually, it takes long CPU time and large memory capacity to solve the PDN circuit consisting of the W-element. Therefore, the first-order Debye rational function is frequently-used to approximate the distributed series impedance (6) and shunt admittance (7):

$$Z(s) = R_0 + sL_0 + \frac{R_1 L_1}{R_1 + sL_1} + \frac{R_2 L_2}{R_2 + sL_2} + \frac{R_3 L_3}{R_3 + sL_3} + \cdots, \tag{10}$$

$$Y(s) = G_0 + sC_0 + \frac{G_1C_1}{G_1 + sC_1} + \frac{G_2C_2}{G_2 + sC_2} + \frac{G_3C_3}{G_3 + sC_3} + \cdots \quad (11)$$

From Eq.(10) and (11), the frequency-dependent unit cell model can be derived as illustrated in Fig. 5(c). In Fig. 6(c), the number of RL parallel networks at the portion of the distributed series impedance is determined from the number of poles of Eq. (10). the number of GC series networks is also determined from the number of poles of Eq. (11).

The unknown parameters of the Debye functions, such as R_i, L_i, G_i, and C_i (i = 1 ... N), have to be chosen by fitting Eq.(10) and (11) to sampled-data calculated by Eq. (6) and (7). This procedure can be performed by several fitting and optimizing routines, such as the fitting functions in the MathWorks MATLAB and vector-fitting algorithm [10], et al. For example, we obtained the first-order Debye model as shown in Fig. 7. In this example, the dimensions and medium coefficients of the unit cell are w=2.5mm, d=0.2mm, t=0.03mm, σ_c =5.8×107, ε_r=4.5 and tan(δ)=0.02. Fig. 8 indicates that there is a good correlation between the Debye model and analytical data.

B. LIM simulation

In [8], the first-order Debye model of high-speed interconnects was solved by a LIM-like leapfrog time stepping scheme. However, as has been mentioned, LIM scheme has a limitation of the circuit structure to be analyzed. Every branch must have an inductor and every node must be connected with the grounded capacitor. The Debye model as illustrated in Fig. 7 does not meet these conditions. Therefore, in order to obtain I_{ij} from V_i and V_j, every first-order Debye model of the distributed series impedance had to be solved via matrix inversion in [8]. Also the shunt admittance has to be solved in a similar manner. This procedure is an inefficient even if LIM is used.

In this paper, we propose an effective modeling of frequency-dependent parameters for LIM simulation. In our method the RL parallel network is transformed into RL series network. From Eq. (10), the KVL is given by:

$$V_i - V_j = \left(R_0 + sL_0 + \sum_{m=1}^{4} \frac{R_m L_m}{R_m + sL_m} \right) I_{ij} \quad (12)$$

Next, Eq. (12) can be rewritten as

$$(V_i - V_j) \sum_{m=1}^{5} \frac{k_m}{s - p_m} = I_{ij} \quad (13)$$

where,

$$(V_i - V_j) \frac{k_m}{s - p_m} = I_{ij,m} \qquad (m = 1, \cdots, 5) \quad (14)$$

From Eq.(14), each parameter of the RL series network can be obtained from:

$$V_i - V_j = \frac{s - p_m}{k_m} I_{ij,m} = (sL_{ij,m} + R_{ij,m}) I_{ij,m} \quad (15)$$

In our method, the GC series network is also transformed into GC parallel network in a similar manner. Finally, the procedure of our transformations is summarized in Fig. 9. Through this transformation, we do not have to perform any matrix inversions. For instance, we can obtain $I_{ij^{\circ}m}$ from V_i and V_j using only Eq.(15) even in time-domain.

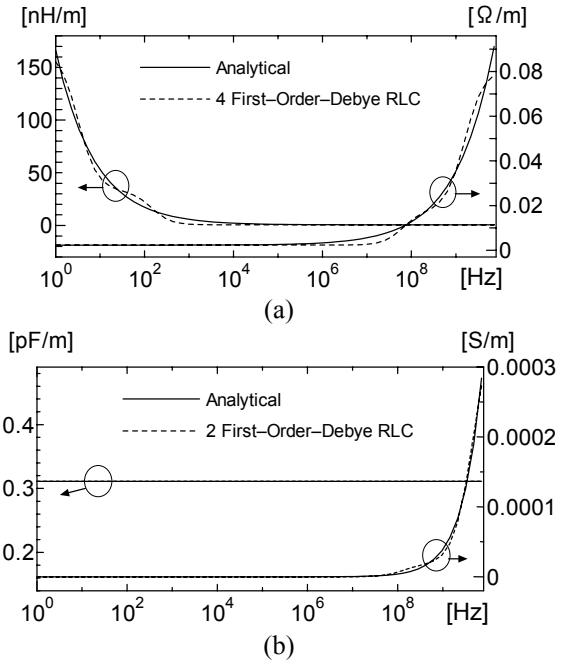

Fig. 8. Characteristics of Frequency-dependent parameters. (a) R(orms/m) and L(H/m). (b) G(S/m) and C(F/m).

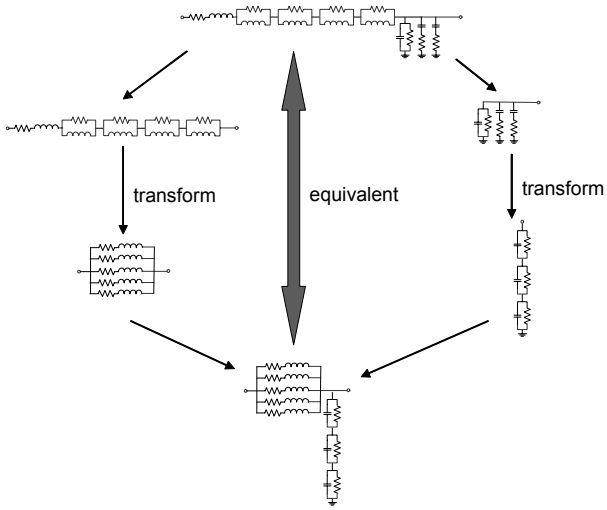

Fig. 9. Transformation of the first-order Debye model.

V. Numerical Results

First of all, in order to verify the efficiency of our parallel-distributed LIM algorithm, we simulated a transient response of a power/ground plane, as illustrated in Fig. 10, using 1PE and 2PE. The source point was excited with a Gaussian pulse. All simulations were performed on Intel Pentium M 1.7GHz personal computer. From Fig. 11, the voltage fluctuations at the observation point (60cm × 60cm) show the good agreement between results using 1PE and 2PE. Furthermore, Table 1 indicates that the CPU time of the 2PE simulation is almost half of the 1PE's CPU time.

Next, we simulated a power/ground plane which has frequency-dependent properties as illustrated in Fig. 12. The source point P01 was excited with a triangular waveform. All simulations were performed on SUN Blade Workstation. To verify our modeling validity and efficiency, we compared the transient responses simulated using the Star-Hspice and our LIM simulator. From Fig. 13, our first-order Debye model can be correctly solved by the LIM simulator. From Table 2, our LIM simulation is fastest among all simulations.

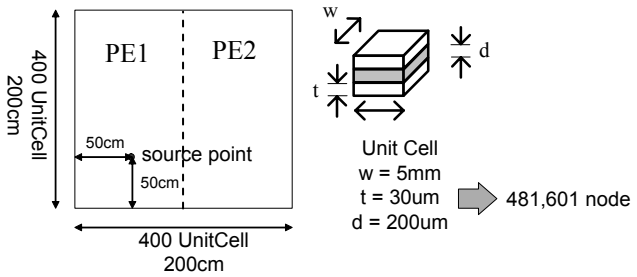

Fig. 10. First example of power/ground plane.

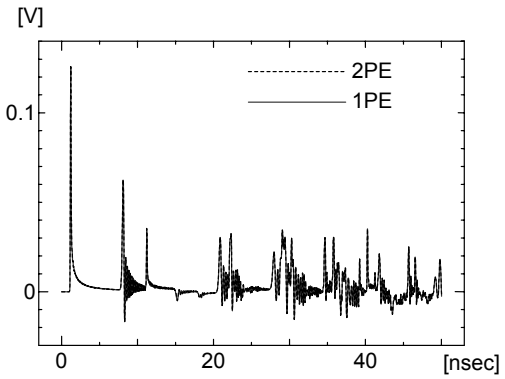

Fig. 11. Transient responses of the observation point (60cm × 60cm) in the first example.

Table 1: The CPU time comparisons of the first example.

Number of PE	CPU Time (sec)
1	110.3
2	57.5

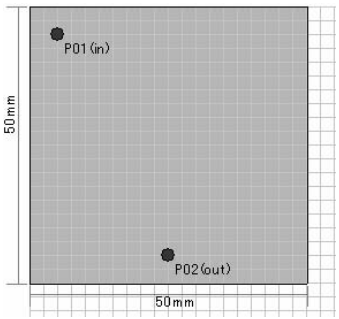

Fig. 12. Second example of power/ground plane.

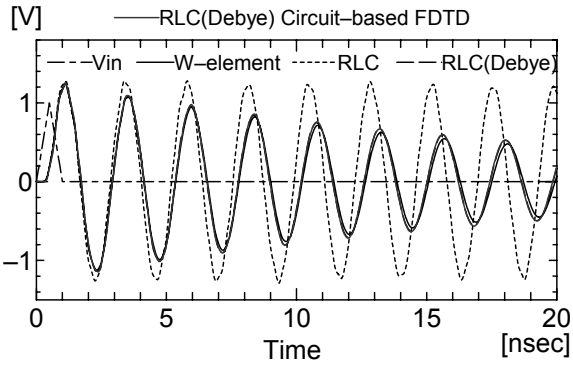

Fig. 13. Transient responses of the observation point P02 in the second example.

Table 2: The CPU time comparisons of the second example.

Simulator	Star-Hspice			LIM
Model	RLC	Debey	W-element	Debey
Problem Size	1282 nodes	5524 nodes	442 nodes	400 unit cells
CPU Time (sec)	3.3	19.7	365.6	0.47

VI. Conclusions

In this paper, we proposed the parallel-distributed LIM algorithm and an effective modeling of frequency-dependencies of the PDNs to solve by LIM. From the numerical results, it is obvious that the parallel computation is very efficient for the LIM algorithm. Also our transformed Debye model is quite effective to the LIM simulation.

In the future work, we have to consider the optimal partitioning of any irregular shaped power/ground plane for parallel computing in case of using many PEs.

Acknowledgements

This work was supported, in part, by Semiconductor Technology Academic Research Center (STARC), Japan. The authors would like to thank to Dr. K. Mashiko,

STARC, Mr. G. Yokomizo, Renesas, Mr. M. Utsuki, Sony, Mr. S. Hatasa, ROHM, for their useful suggestions and comments.

References

[1]. T. Watanabe and K. Srinvasan, H. Asai, M. Swaminathan, “Modeling of Power Distribution Networks with Retardation Using the Transmission Matrix Method,” *Proc. IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEP)*, pp.233-236, Oct. 2004.

[2]. L.D. Smith, R. Anderson, and T. Roy, “Power Plane SPICE Models and Simulated Performance for Materials and Geometries, ” *IEEE Trans. Advanced Packaging*, vol. 24, no. 3, pp.277-287, Aug. 2001.

[3]. J. E. Shutt-Ainé, “Latency Insertion Method (LIM) for the Fast Transient Simulation of Large Networks,” *IEEE Trans. Circuits and Systems-I*, vol. 48, no.1 pp. 81-89, Jan. 2001.

[4]. Z. Deng and J. E. Schutt-Ainé, “Stability analysis of latency insertion method (LIM),” *Proc. IEEE 13th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 167-170, 2004.

[5]. K. S. Yee, "Numerical Solution of Initial Boundary Value Problems Involving Maxwell's Equations in Isotropic Media," *IEEE Trans. Antennas Propagat.*, 14, 4, pp.302-207, 1966.

[6]. T. Watanabe and H. Asai, “Synthesis of time-domain models for interconnects having 3-D structure based on FDTD method”, *IEEE Trans. Circuits and Syst. –II*, vol. 47, no. 4, pp. 302-305, April 2000.

[7]. T. Watanabe, H. Asai, T. Sasaki, and K. Araki, “Parallel-Distributed FDTD-Based Full-Wave Simulator for Large-Scale Printed Wiring Boards,” *Proc. IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEP)*, pp.287-290, Oct. 2002.

[8]. Alberto Scarlatti and Christopher L. Holloway,”An Equivalent Transmission-Line Model Containing Dispersion for High-Speed Digital Lines—With an FDTD Implementation”, *IEEE Trans. Electromagnetic Comp.*, vol. 43, no. 4, Nov. 2001

[9]. H. Kubota, Y. Tanji, T. Watanabe, and H. Asai , “Generalized Method of the Time-Domain Circuit Simulation based on LIM with MNA Formulation”, *Proc. The IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2005, in press.

[10]. B. Gustavsen and A. Semlyen, “Rational approximation of frequency domain responses by vector fitting,” *IEEE Trans. Power Delivery*, vol. 14, no. 3, pp. 1052-1061, July 1999.