Yield-Preferred Via Insertion Based on Novel Geotopological Technology

Fangyi Luo
Department of Computer Engineering
University of California at Santa Cruz
Santa Cruz, CA 95064
luofy@soe.ucsc.edu
Tel:408-844-8558
Fax:408-844-8566

Yongbo Jia
Nannor Technologies, Inc.
4699 Old Ironsides Dr., STE 270
Santa Clara, CA 95054
jiayb@nannor.com

Wayne Wei-Ming Dai
Department of Computer Engineering
University of California at Santa Cruz
Santa Cruz, CA 95064
dai@soe.ucsc.edu

Yield-preferred via insertion is an effective method to reduce the yield loss caused by via failures. The existing methods to apply the redundant-cut vias in metal layers are not efficient nor adequate. In this paper, we present an effective and efficient yield-preferred via insertion method based on a novel geotoplogical layout platform, GEOTOP. Our method chooses the most yield-favored via candidate and insert it into the layout without causing any design rule violations. Experiments with real industry designs show that our method can achieve very high rate of yield-preferred via without increasing the design die size within acceptable running time.

I. Introduction

As the feature size of integrated circuit continues exponentially scaling down, many new problems appear in recent process generations [1]. These new problems make it a very hard task for both designers and foundries to maintain high yield as the design size grows up. Among them, one of the most important is the yield loss due to via open failures.

Via is the component in VLSI designs to connect metal wires on different metal layers. Via open failure may occur, causing unwanted loss in yield and performance. A complete via open failure will lead to a complete broken net, which will fail the entire design. A partial via open failure will increase the resistance of the interconnect on the signal net and bring undesired delay and damage the performance. As the VLSI feature size continues shrinking to deep sub-micron regime, vias become more and more sensitive to various variations, such as cut misalignment, electron migration and thermal stress induced voiding [2] [3]. In this background, yield loss due to via open failure becomes more and more important and requires better control.

Several types of yield-preferred vias were proposed to reduce the yield loss caused by via failures [2][4]. One of the most talked about type is the redundant-cut via. A redundant-cut via is a via with 1 or more redundant cuts which are not required in functionality but will greatly reduce the chance of the via open failure. Another one is the fat via, which is a via with enlarged metal coverage. Some major foundries [5] are already recommending the massive usage of yield-preferred vias in their 130nm and 90nm processes to their customers for better yield. And it is likely that a certain rate of yield-preferred vias will be a required rule in the more advanced processes.

How to use yield-preferred vias in designs becomes a new challenge. Several EDA tool vendors claim that their latest products, such as [6][7], can apply redundant-cut vias in the layouts, while the fat vias are seldom spoken of. Even only dealing with redundant-cut vias, they can not do it well. These tools can be classified into two categories: detail router based tools and GDSII based tools. It seems like a good choice to apply yield-preferred vias at the detail routing stage. However, the yield-preferred vias need more die area and make routing problem more complicated. The routers' built-in grid-base nature has limited their ability to exploit the routing resource thoroughly. On the other hand, it is very hard for the routers to make the online decisions, such as where to use the yield-preferred vias, which via is the most yield preferred, since the whole layout routing has not been finished yet. Therefore, the routers will encounter either a low insertion rate or a loss of routable nets when trying to insert yield- preferred vias. Xu's [4] effort with maze router has achieved a redundant-cut via rate around 65% with a non-negligible loss (10%) of routable nets, which is not acceptable for industry applications. More die size area will be required as the cost for a better redundant-cut via rate and less loss of routable nets. After all the major task of the router is to determine the paths in a limited area for as many nets as possible. Cadence Nanoroute, for example, belongs to this category. On the other hand, the GDSII based tools work on GDSII files. They look around polygons and replace single-cut vias with redundant-cut vias. However, due to the huge size of GDSII data, they are very slow. Furthermore, since they are working at a post tapeout stage, their ability is quite limited so that they can only achieve a relatively lower rate. Even worse, it is almost impossible to feed their result back to earlier design stages for verification and further optimization. Sagantec SiFix, for example, belongs to this category.

In this paper, we step further and propose a new post-layout yield-preferred via insertion method based on a novel GEOTOPological layout encoding platform, GEOTOP. Our method selects the most yield favored via according to the context and insert it into the layout. GEOTOP can achieve a very high yield-preferred via rate without sacrificing the routable nets in the given routed design. This method also provides the option for designers to keep selected nets untouched, which is desired by designers to minimize the disturbance on the design due to the insertion of the yield-preferred vias.

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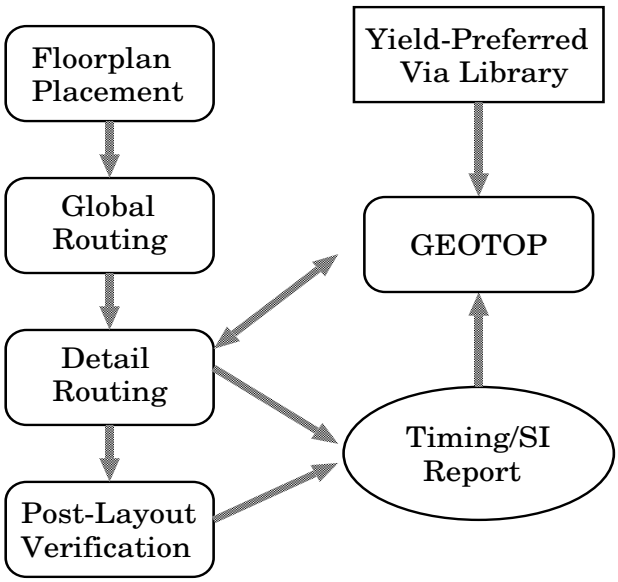

Fig. 1. Geotopological layout optimization platform in the major design flow

II. Method Overview

Our motivation is very straightforward. Since the major task for the routers is to solve the problem of routability, just let them focus on producing a routed layout with the limited routing resource. After a valid layout is generated, we insert the most yield-favored vias wherever applicable in the layout.

We use industry standard exchange files for input and output. Different from the GDSII based tools which work in the post tapeout stage, GEOTOP works in the post routing stage. Our results can be fed back to the routers for more operations. The designer can iterate between the router and GEOTOP until a satisfactory result is achieved. Figure 1 shows the position of GEOTOP in the major design flow.

Figure 2 illustrates our method to insert yield-preferred vias. Given a routed metal layout with geometrical routing paths, we transform it into a geotopological layout in which the geometrical paths of unmodifiable nets are recorded and the paths of modifiable nets are extracted to topological equivalent paths. A yield-preferred via candidate list is created with a priority order according to the yield preference. For each modifiable normal single-cut via, the candidate list is scanned to get the most yield-favored via to insert into the layout without introducing any design rule violations. Finally, a fast geometrical engine produces the optimized geometrical wiring layout according to the geotopological layout with the yield-preferred vias. The following section will give more details.

III. Method details

This section will give more details on our geotopological platform, GEOTOP, yield-preferred vias selection/insertion and the geometrical engine which produces the optimized layout.

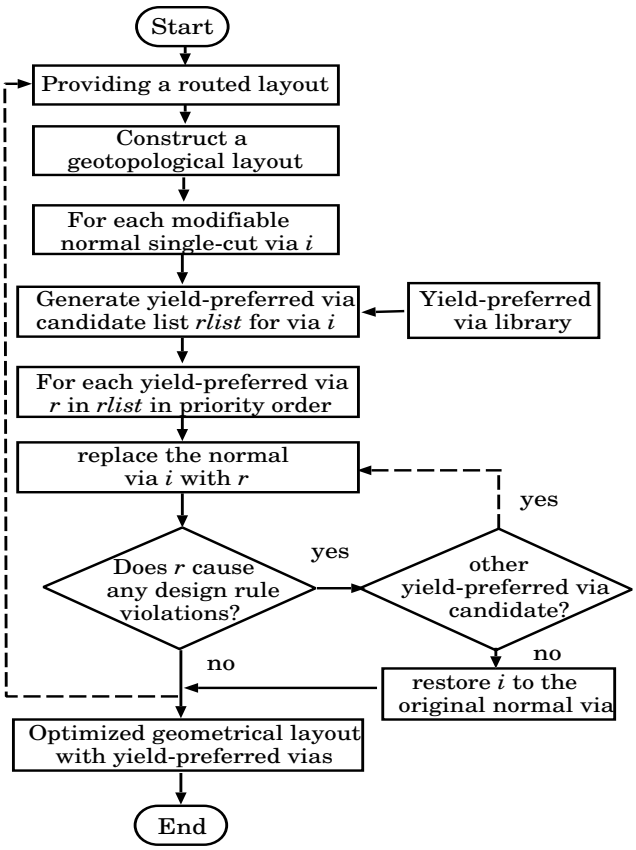

Fig. 2. Yield-preferred via insertion flow

A. Geotopological Technology

Topological layout representation technologies were developed in the last decade for various purposes [8][9][10]. TEG [11] is the first post-layout optimization system based on the topological layout representation. The topological layout only captures the relative positions and connections of the layout elements. This built-in nature makes this technology very flexible in modifying routed layouts. However, since there is no geometrical information of the wires kept in the topological layout, it may suffer from the inconsistency with the original geometry layout. Furthermore, it may change wiring paths which the designers want to keep untouched, such as timing critical nets, etc. Based on the concerns above, we developed our new geotopological technology.

Our new geotopological technology is designed to keep the power of topological technology for post-layout optimization and, at the same time, avoid the shortcomings by keeping the necessary geometrical information from the original geometrical layout.

The necessary geometrical information may be included in a ”hard” net list which comes along with the routed design. The designers can put the nets they want to keep untouched in the list, for example:

- Timing critical nets. Any change in the wiring path or the wire length of these timing critical may result in the timing failure of the design. These nets should be kept unchanged absolutely.

- The nets specified by customers. Some patterns in the layout may be designed according to some certain requirements, such as antenna rule. The designers will, of course, hope to keep these features.
- Sometimes, the designers only want a local optimization in a specified area or an optimization among several specified nets. Extracting the whole layout to topological layout and optimization will be highly costly and risky. The uncertainty introduced may demand for extra ECO loops and longer design-to-market time. In this case, all the nets which are NOT specified for optimization will be ”hard” nets and kept untouched.

Given a routed layout, TEG uses the vias and the corners of the boundary as the vertices of the triangles to encode the whole layout. Each wiring path is represented by the sequence of the triangle edges it goes across and the relative position with other wiring paths on each triangle edge it goes across. This encoding only captures the topological information of the layout. The geometrical information which is necessary and critical may be totally lost.

In our geotopological method, GEOTOP first goes through the wiring paths of the nets in the ”hard” net list when importing a routed design. In the geotopological layout, every segment of the ”hard” wiring path is exactly the same as in the original geometrical layout. All the wiring paths of the nets not in the ”hard” net list are represented topologically. In this way, all unmodifiable nets defined in the list are represented by their respective geometrical wiring paths while all other nets are simultaneously represented by their respective topological wiring paths which are extracted from the initial geometrical layout. Given a routed design, every metal layer is processed and a corresponding geotopological layout is generated. Figure 3 gives a pair of the original geometrical layout and the corresponding geotopological layout. In the example, the solid geometrical wiring paths stand for the wiring paths of the nets in the ”hard” net list.

In the following section, we will describe how we insert the most yield favored vias into the geotopological layout.

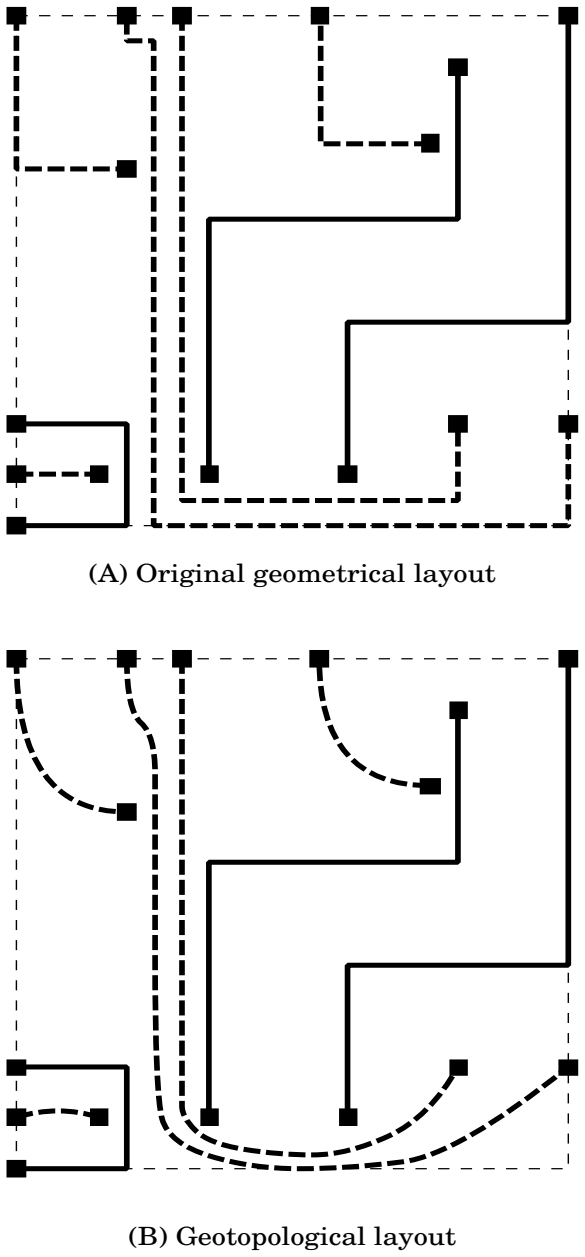

Fig. 3. (A) Original geometrical layout (B) Equivalent geotopological layout

B. Yield-preferred Vias Insertion

Based on the geotopological encoded layouts, yield-preferred vias are inserted according to applicable design rules, leaving the unmodifiable nets intact.

Referring back to Figure 2, a yield-preferred via candidate priority list is generated for each normal single-cut via which is modifiable. A yield-preferred via is a via with a certain geometrical shape configuration. Figure 4 gives the examples for a fat single via, a normal redundant-cut via and a fat redundant-cut via. Different geometrical shape configuration will result in different yield influence on the layout. In the fat vias, the enlarged metal covering over the cut will reduce the yield loss caused by misalignment. The redundant-cut vias will greatly reduce the chance of net breaking fault caused by via open failure. From the manufacturability viewpoint, the fat redundant-cut via has the least possibility of via break failure and the best yield improvement, followed by the normal redundant-cut via, and then the fat single via. On the other hand, for a specified normal single-cut via, different insertion direction of the

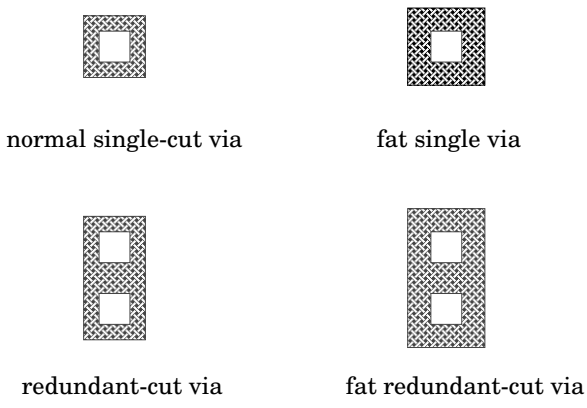

Fig. 4. Yield-preferred vias: fat single via, normal redundant-cut via and fat redundant-cut via

redundant-cut via also has different disturbance on the layout [12]. Figure 5 illustrates a group of possible redundant-cut vias insertion direction for replacing a normal single-cut via which connects to two metal layers, M1 and M2. M1 is the lower metal layer in the vertical preferred routing direction. M2 is the upper metal layer in the horizontal preferred routing direction. Via A, B, C are in the vertical direction. Since M1 is in vertical direction and M2 is in horizontal direction, these three placements cause more changes in M2 layer than in M1 layer. For the same reason, Via D, E, F will cause more changes in M1 layer then in M2 layer. Since M1 is the lower layer, A, B, C have higher priority than D, E, F. Among Via A, B and C, A brings the least disturbance to M1, C brings the most. Therefore, A is the most yield-preferred, followed by B, and then C. For the same reason, we have the priority order of D, E, F. Every redundant-cut via has a fat version with a higher priority. Therefore, we have 6 fat redundant-cut vias with the highest priority, and 6 normal redundant-cut vias, plus 1 fat single-cut via with the lowest priority, 13 yield-preferred vias in total in the candidate list.

Please note that our configuration of the yield-preferred via candidate priority list may not be the optimal one. Here in this paper, what we want to present is the concept of the yield-preferred via candidate priority list and the method to insert as many yield-preferred vias into the layout as possible. The designers are strongly recommended to consult with the foundries they are working with to figure out the optimal yield-preferred via candidate priority list.

Referring back to Figure 2, after the yield-preferred via candidate list is generated for a specified modifiable normal single via, the normal single via is replaced with the yield-preferred via from the candidate list with the highest priority. Replacing a normal single via with a redundant via would cause changes on both metal layers. A incremental geotopological design rule checker then checks the affected area for design rule violations in the 2 relevant geotopological layouts. If the replacement does introduce new design rule violations, another attempt is made to replace this normal single via with the next yield-preferred via in the candidate list. If not, the current yield-preferred via replaces this normal single via and the process goes back to replace the next normal single modifiable via. In the situation that every yield-preferred via in candidate list would cause design rule violations, the original via will not be changed.

C. Optimized Geometrical Layout

After all modifiable normal single-cut vias have been processed and replaced with yield-preferred vias where applicable, the geometrical engine produces the optimized geometrical layouts according to the geotopological layouts with the yield-preferred vias.

This geometrical optimization engine is derived from a previous studied topology-to-geometry transformation engine [13]. In geotopological layout, the "hard" wire paths are kept as their original geometrical paths. When producing the optimized geometrical layout, the geometrical engine sweeps through the geotopological layout and optimizes the geometrical wiring path for each wiring segment one by one. The optimized paths of the "hard" wiring paths are directly copied from the geotopological representation, while those of the other wiring paths are adjusted according to the nearby geometrical shapes. Another improvement is a net-based spacing rule lookup table. The spacing rule lookup table enables the engine to optimize the valid geometrical layout following a complex rule set. The spacing rule lookup table is developed at the time the original layout is read, recording the special spacing rules other than the minimum spacing requirement. When producing the optimized geometrical layout, the lookup table is referred for the spacing requirement between the specified nets.

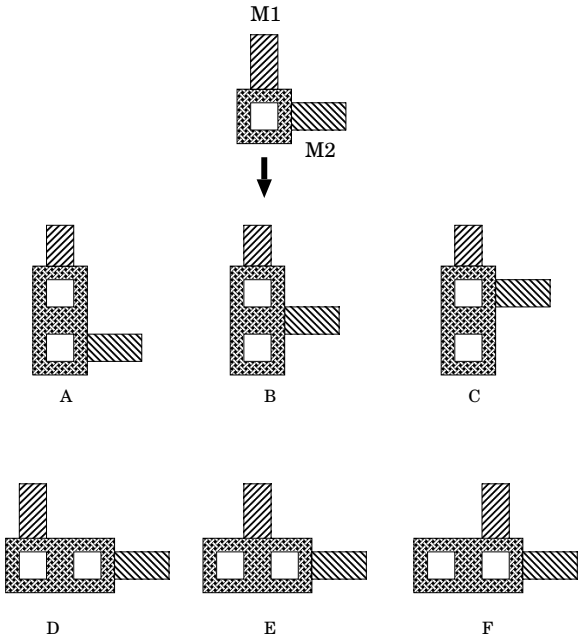

Fig. 5. Redundant-cut vias in different directions

After an optimized geometrical layout has been produced for each metal layer, the engine exports an exchange file in industry standard which has all the geometrical information in the design, including all the yield-preferred vias. The designers can feed this exchange file back to routers for more operations or as the input for the next design stage.

IV. Experiment Results

All the experiments are running on a Linux machine with 2 P4 2.8G CPUs and 2G memory. We choose our test cases from industry with different sizes. Table I shows the list of a group of our test cases. Column 1 of Table I shows the number of routing layers of each design. Column 2 and Column 3 give the number of the nets and the number of the gates in each design, giving a basic concept of size of the designs. Column 6 gives the overall yield-preferred via insertion rate of the design.

In this group of experiments, we input each routed design, insert yield-preferred vias into the routing layers, then produce the optimized wiring paths in the routing layer and output the design in the same format. To make a comparison with other methods, the yield-preferred vias are chosen from the 6 normal redundant-cut vias. The usage of the 6 fat redundant-cut vias will slightly lower the insertion rate, since they are using

TABLE I
YIELD-PREFERRED VIA INSERTION RATE

Design	# of routing layers	# of nets	# of gates	# of total vias	# of yield-preferred vias	yield-preferred via rate
case1	2	5k	22k	25.1k	24.2k	96.4%
case2	3	7.8k	35k	45k	40.2k	89.3%
case3	4	15k	44k	74.7k	68.0k	91.4%
case4	4	17k	58k	87.3k	80.8k	92.6%
case5	3	24k	83k	149.1k	143.1k	95.95%
case6	3	37.8k	285k	280.1k	251.5k	89.8%
case7	7	64.7k	256K	890.8k	813.2k	91.3%
case8	3	115k	1020k	1146k	1028k	89.7%

more area. When importing each design, the PrimeTime report is also imported to identify the timing critical nets and freeze them. These timing critical nets are treated as "hard" nets, their geometrical wiring paths are kept unchanged during the whole optimization. We use commercial DRC tools from major EDA tool vendors to check through the optimized layouts GEOTOP produced to ensure they have no design rule violations.

Our experiments show a very high yield-preferred via insertion rate. Compared with Xu's experiments [4], our experiments use real industry designs which are not randomly generated. We get a much higher insertion rate. Even in the design with the highest metal density, our method still achieves a rate over 89%. Please keep in mind that we didn't increase the die size area nor sacrifice even a single routable net when achieving these impressive insertion rates. Our method is also very fast. For case 8, a 1 million gate design, the total turn-around time is around 1 hour and a half.

Figure 6 and Figure 7 give a pair of example of the original layout and the layout after yield-preferred via insertion in test case 6. Two metal layers are displayed in the figures.

We have another experiment with test case 9. It is also a real industry design with 148k nets and 1.2M gates in 90nm technology. The total number of vias is about 1.2M. The original routing is generated by some major commercial detail router with redundant-cut via option. The original redundant-cut via rate is about 58%. First, we directly insert normal redundant-cut vias into the original layout. We get 92k more redundant-cut vias, the rate rises to 66%. We make another attempt by restoring the redundant-cut vias in the original layout back to normal single vias and then inserting the redundant-cut vias into the layout through GEOTOP. The rate jumps to 84%, which is about 310K MORE redundant-cut vias than the commercial router without increasing die size or loss of routable nets. According to Poisson yield model [14], 2,000,000 more vias in a design with an average rate of 5 break failures per 1 billion cuts, which is a very realistic data, will bring at least 1% yield improvement. If scaled up to multi-million gate design, our result will bring significant yield enhancement.

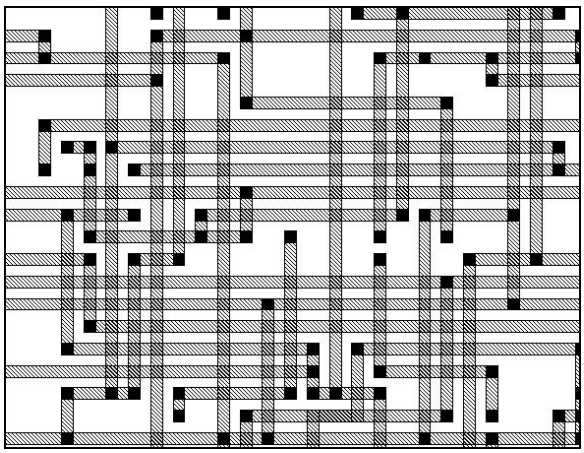

Fig. 6. Original layout without any yield-preferred vias

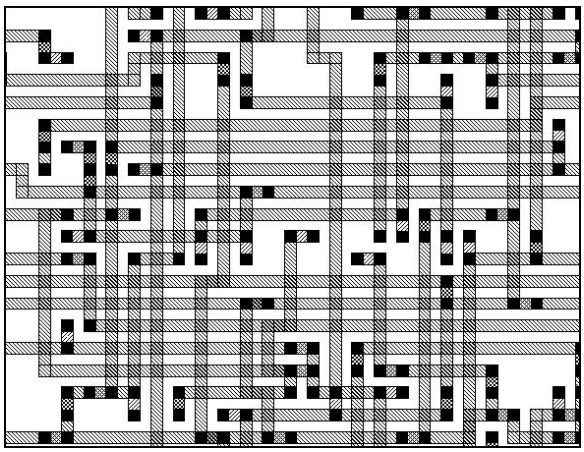

Fig. 7. Optimized layout with yield-preferred vias

V. CONCLUSION

In this paper, we present a yield-preferred via insertion method based a novel geotopological platform, GEOTOP. The objective layout is first extracted to a geotopological layout, then the most suitable yield-preferred vias are inserted into the

geotopological layout where applicable, finally the optimized geometrical layout is produced. This method guarantees the highest insertion rate and keeps the specified wire paths untouched. Experiments with real industry designs show that over 89% insertion rate can be achieved even in the densest design without introducing any design rule violations, which will bring profitable yield improvement.

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