

## Statistical Corner Conditions of Interconnect Delay (Corner LPE Specifications)

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**Abstract - Timing closure in LSI design becomes more and more difficult. But the conventional interconnect RC extraction method have over-margins caused by its corner conditions settings. In this paper, statistical corner conditions using the independence of variations between process parameters and between interconnect layers are proposed. As a result, the fast-to-slow guardband decreases by half in average, compared to the conventional method. The proposed method is ready for implementation to LPE tools.**

### I. Introduction

Timing closure becomes difficult in LSI design as device scaling proceeds[1]. The demands for reducing over-margin caused by corner condition settings become strong.

An ordinary interconnect RC extraction flow is shown in Fig.1. Firstly, the RC library for various interconnect patterns is generated from the cross-section, once for one technology. On a RC extraction run for a design, the netlist with parasitic RCs is extracted from the layout data by using this RC library. This is generally called LPE (Layout Parameters Extraction). The netlist with parasitic RCs is used for timing verifications in subsequent design steps.

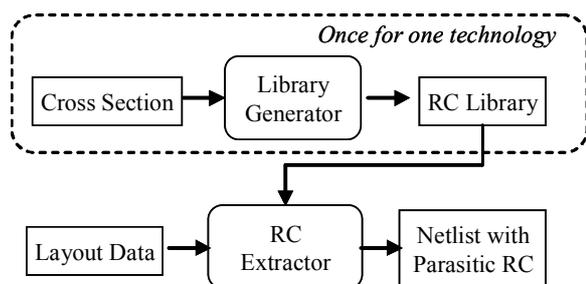


Fig. 1. Ordinary LPE Flow

Recently, the layout pattern dependence of interconnect shape, such as the fluctuation of width and thickness caused by optical proximity effects, an etching process or CMP process, can be taken into account at LPE[2]. This means RC extraction becomes accurate in the center conditions.

In contrast, no effective method has been proposed that determines statistical and accurate corner conditions, because there is not certain knowledge on how to set the variations of the various process parameters statistically to maximize or minimize the propagation delay of signals ( $\tau_{pd}$ ). The details are explained in the next section.

### II. Problems of Conventional Corner Conditions

Fig.2 shows the LPE flow for conventional corner conditions[3],[4]. Two to six cross-sections in which the variations of the process parameters are set to maximize or to minimize  $\tau_{pd}$  are input to the library generator and the RC libraries corresponding to each cross-section are generated. Here, each process parameter is set to be the maximum or minimum value in the variation range. Then the netlists with parasitic RCs corresponding to each library are extracted.

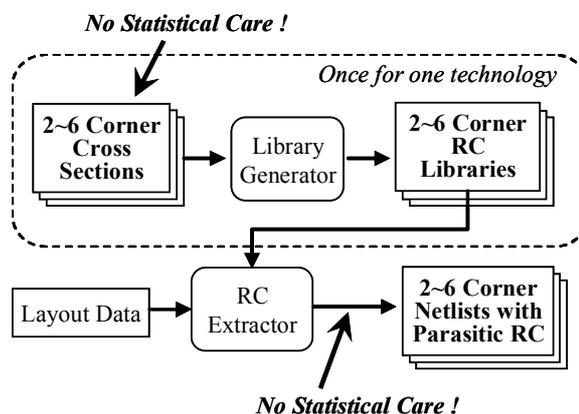


Fig. 2. LPE flow for Conventional Corner Conditions

Surely the timing verification would be accomplished by using the all extracted netlists. But this method is too pessimistic from a statistical viewpoint. As the variations of each process parameter come from different processes, these are independent from each other. Therefore, the corner conditions in which each process parameter is set to be the maximum or minimum value in the variation range are statistically unlikely to happen and the guardband spanning from one corner to another, i.e., fast to slow corners becomes needlessly wide, and causes over-margins.

The same can be applied to the relation between interconnect layers. As different interconnect layers come from different processes, their variations are independent from each other. Therefore, the conventional corner conditions that do not take the statistical independence into considerations is too pessimistic from a statistical viewpoint, and cause over-margins.

These over-margins make timing closure difficult, or enlarge chip sizes, or increase power consumption or waste the performance of the present process technologies. As timing closure, in particular, becomes more and more difficult in recent designs, this situation is fatal.

### III. Method to solve the problems

In this work, the reduction of over-margins caused by the conventional corner conditions is examined from statistical concepts. Here are two concepts:

The first one is the reduction of over-margins by using the independence of the variations of process parameters in a single interconnect layer. It is examined whether the statistical input cross-sections (corner conditions) can be set or not. And a simple method of finding the corner conditions is also examined.

The second one is the reduction of over-margins by using the independence between the variations of interconnect layers. The input cross-sections to be fed in the RC library generator as the corner conditions are constructed from a combination of the corner conditions of involved layers. The resultant output netlists with parasitic RCs would have over-margins. To overcome this, the concept of statistical independence will be applied to the nodes shared with different interconnect layers; the extracted resistances or capacitances will be adjusted appropriately.

#### IV. Statistical Corner Conditions in Single Layer

##### A. Handling of Process Variations

In an interconnect process, the width ( $W$ ), the thickness ( $T$ ), the thickness of insulators ( $D_1$ ,  $D_2$ ) and the dielectric constant ( $\epsilon$ ) are process parameters, as shown in Fig.3. These parameters vary independently because of independent origins, i.e. different process steps.

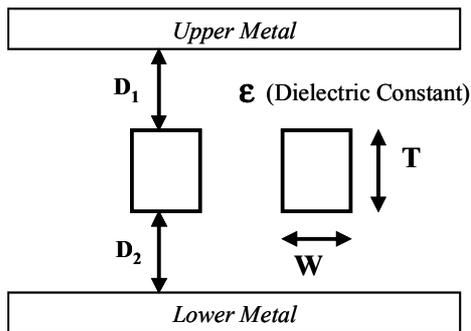


Fig. 3. Process Parameters in Interconnect Cross-Section

Because it is too complicated and impractical to treat all these parameters statistically, target to treat statistically should be limited.  $W$  and  $T$  mainly influence resistance and capacitance, and the other parameters are secondary. The variations of  $D_1$  or  $D_2$  influence the capacitance of interconnects without neighboring interconnects, but signal lines usually have neighboring interconnects. Therefore the ratio of the capacitance to under or upper interconnects in the total capacitance is small. As a result, the influence of the variations of  $D_1$  or  $D_2$  to total capacitance is small. In addition, these secondary parameters can clearly be set to either end of the full variation range to maximize or minimize  $\tau_{pd}$ . Therefore,  $W$  and  $T$  are treated statistically and the secondary parameters are set to be either end of the

full variation range (not statistically). There is another reason. If the secondary parameters also treated statistically, the corner conditions cannot be fixed to limited number. It can be easily understood to extend the statistical examinations on  $W$  and  $T$  described in this paper to these secondary parameters.

##### B. Variations of $R$ & $C$ due to the change of $W$ & $T$

The relation between  $W$  variations and  $T$  variations is shown in Fig.4. The x-axis is  $\Delta W/\sigma(W)$ , and the y-axis is  $\Delta T/\sigma(T)$ . The variation ranges are set to  $\pm 3\sigma$  here (as an example), but these can be set to any value at a designer's discretion.

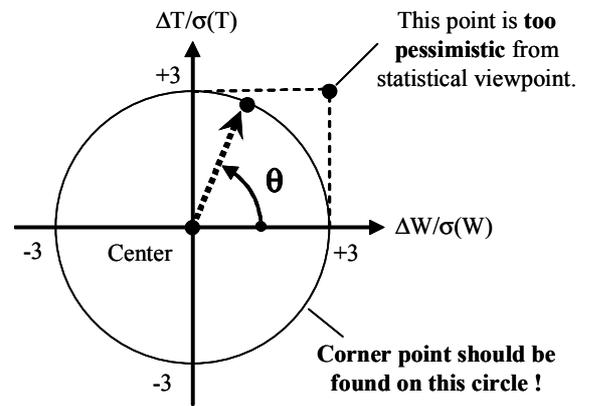


Fig. 4. Variations of  $W$  &  $T$

It is pessimistic to set both  $W$  and  $T$  to the maximum or the minimum and it is sufficient to find the corner points on the circle  $((\Delta W/\sigma(W))^2 + (\Delta T/\sigma(T))^2)^{1/2} = 3$  from a statistical viewpoint. It matters whether the point that maximizes or minimizes  $\tau_{pd}$  can be fixed on this circle or not.

Firstly, the resistance and capacitance variations simulated by TCAD for various  $\theta$  along the circle are shown in Fig.5 and Fig.6. The target is a local interconnect of a 90nm CMOS process. The interconnect pitch was varied when the upper and lower interconnects exist (Case1) or not (Case2). The x-axis is  $\theta$ , and the y-axis is the ratio to the center condition.

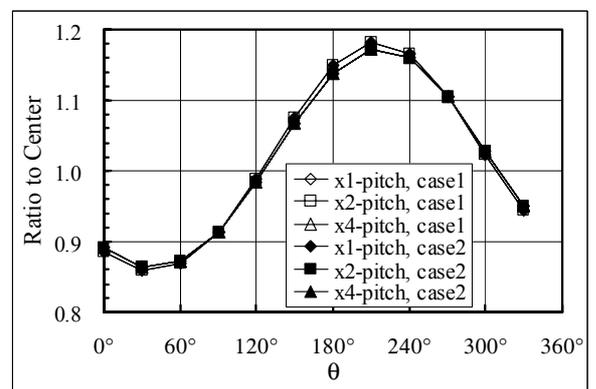


Fig. 5. Resistance Variation

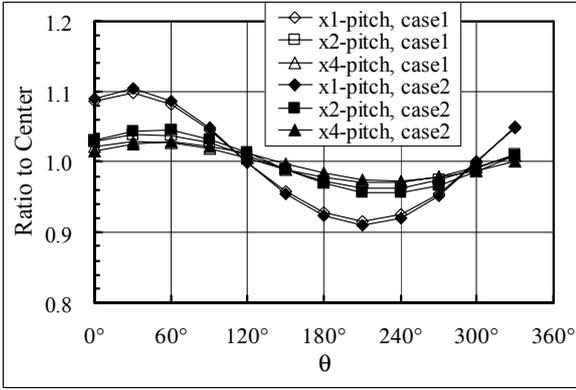


Fig. 6. Capacitance Variation

It can be seen that the resistances are minimized and the capacitances are maximized at  $\theta=30^\circ$ , and the resistances are maximized and the capacitances are minimized at  $\theta=210^\circ$ . These results are reasonable because resistances are maximized when the sectional area of the interconnect is minimized and capacitances are minimized in the same case. Note that  $\theta$  maximizing or minimizing capacitance doesn't change for all interconnect pitches or cases.

C.  $\tau_{pd}$  Variations due to the change of  $\theta$

The variations of  $\tau_{pd}$  with respect to  $\theta$  are analyzed. Various inverter chains were simulated and  $\tau_{pd}$  per one stage was measured. The inverter chains were loaded with interconnect of various patterns and lengths. The inverter size was also changed.

Fig.7 shows the inverter size dependence of the  $\tau_{pd}$  variations. The interconnect length is fixed at 2mm and the interconnect pattern is fixed to the minimum pitch of Case2.  $\tau_{pd}$  is maximized at  $\theta=30^\circ$  and minimized at  $\theta=210^\circ$  when the inverter is smaller. Oppositely,  $\tau_{pd}$  is minimized at  $\theta=30^\circ$  and maximized at  $\theta=210^\circ$  when the inverter is larger. It is remarkable that  $\tau_{pd}$  is always minimized or maximized at  $\theta=30^\circ$  or  $\theta=210^\circ$  in any case. In this case, it can be observed that the variations of  $W$  and  $T$  do not change the delay with X4-size inverter.

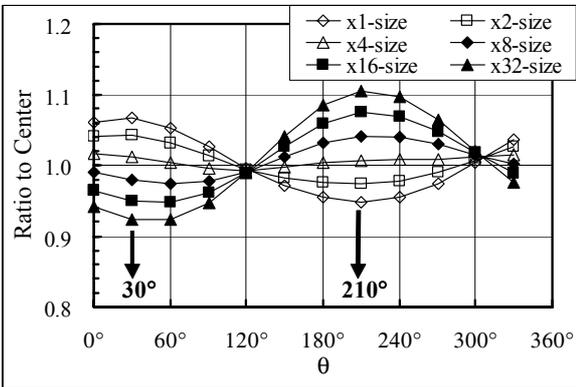


Fig. 7.  $\tau_{pd}$  Variation (Inverter Size Dependence)

Fig.8 shows the pattern dependence of  $\tau_{pd}$  variations. The inverter size is "x2" and the interconnect length is fixed at 2mm.  $\tau_{pd}$  is maximized at  $\theta=30^\circ$  and minimized at  $\theta=210^\circ$  when the interconnect pitch is smaller.  $\tau_{pd}$  is minimized at  $\theta=30^\circ$  and maximized at  $\theta=210^\circ$  when the interconnect pitch is larger. Whether the upper and lower interconnects exist or not does not change the essence of the results. Also in this case,  $\tau_{pd}$  always minimized or maximized at  $\theta=30^\circ$  or  $\theta=210^\circ$ .

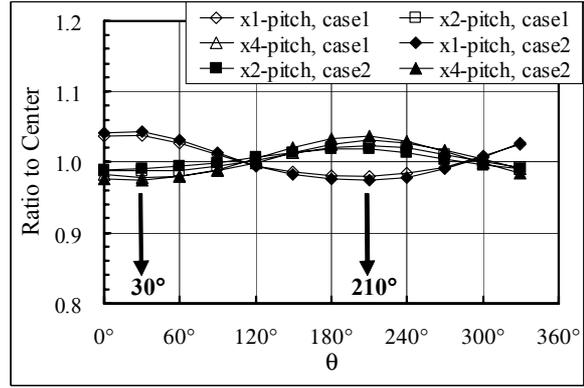


Fig. 8.  $\tau_{pd}$  Variation (Interconnect Pattern Dependence)

Fig.9 shows the interconnect length dependence of  $\tau_{pd}$  variations. The inverter size is "x1" and the interconnect pattern is fixed to minimum pitch in case2.  $\tau_{pd}$  is maximized at  $\theta=30^\circ$  and minimized at  $\theta=210^\circ$  in all cases.

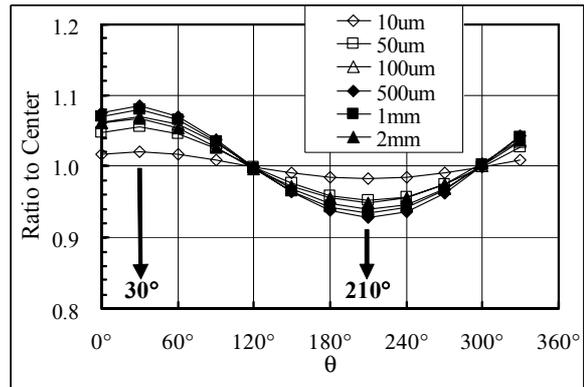


Fig. 9.  $\tau_{pd}$  Variation (Interconnect Length Dependence)

D. Summary of  $\tau_{pd}$  Variations

From the results above, it is understood that  $\tau_{pd}$  is always minimized or maximized at  $\theta=30^\circ$  or  $\theta=210^\circ$ . This means that the corner conditions of this local interconnect layer are limited to two cases only ( $\theta_1=30^\circ$  and  $\theta_2=210^\circ$ ).

This can be explained as follows. Resistance and capacitance govern  $\tau_{pd}$ . Each of them varies alternately in the opposite phase with respect to  $\theta$ . As either of them mainly governs  $\tau_{pd}$  in any case,  $\theta$  maximizing or minimizing the resistance or capacitance ultimately maximizes or minimizes  $\tau_{pd}$ .

For a semi-global interconnect layer of a 90nm CMOS process, either of  $\theta=60^\circ$  or  $\theta=240^\circ$  is found to be the corner condition from a similar analysis. The reason why the  $\theta$  that achieve corner conditions is different from the local interconnect layer is the difference of the aspect ratio and the difference of the ratio of W or T variation ranges to W or T themselves.

E. Determination method of Corner Conditions ( $\theta_1$  and  $\theta_2$ )

The above examinations are detailed to show the validity of the method. But it can be understood from these examinations that only the resistance (or capacitance) simulations with varying  $\theta$  are necessary to find the  $\theta$  maximizing or minimizing resistance (or capacitance), and these are the corner conditions ( $\theta_1$  and  $\theta_2$ ). Therefore, the corner conditions can be automatically found by improved LPE tools.

F. Statistical Corner Conditions with All Parameters

As already mentioned, the secondary parameters (except for W and T) are set to the either end of the full variation range to maximize or minimize  $\tau_{pd}$ . The thickness of insulators among layers ( $D_1, D_2$ ) are set to the maximum in the fast corner conditions, and the minimum in the slow corner conditions. On the other hand, the dielectric constant ( $\epsilon$ ) is set to the minimum in the fast corner conditions, and the maximum in the slow corner conditions. In addition, the resistance of via ( $R_{via}$ ) is set by the similar way. After all, as these parameters should be set to both ends to each corner of W and T ( $\theta_1$  and  $\theta_2$ ), it ends up with  $2 \cdot 2 = 4$  corner conditions (Fig.10 and TABLE I).

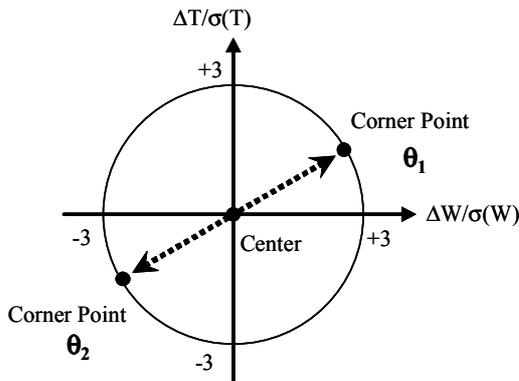


Fig. 10. Statistical Corner Conditions ( $\theta_1$  and  $\theta_2$ )

TABLE I  
Statistical Corner Conditions with All Parameters

Corner Conditions	W	T	$D_1, D_2$	$\epsilon$	$R_{via}$
RCmax	$3\cos(\theta_2) \sigma$	$3\sin(\theta_2) \sigma$	$-3\sigma$	$+3\sigma$	$+3\sigma$
Cmax	$3\cos(\theta_1) \sigma$	$3\sin(\theta_1) \sigma$	$-3\sigma$	$+3\sigma$	$+3\sigma$
RCmin	$3\cos(\theta_1) \sigma$	$3\sin(\theta_1) \sigma$	$+3\sigma$	$-3\sigma$	$-3\sigma$
Cmin	$3\cos(\theta_2) \sigma$	$3\sin(\theta_2) \sigma$	$+3\sigma$	$-3\sigma$	$-3\sigma$

The names of the corner conditions RCmax or RCmin signify that these conditions maximize or minimize R·C. The names of the corner conditions Cmax or Cmin signify that these conditions maximize or minimize C. In general, RCmax and RCmin become the corner conditions for long interconnects, and Cmax and Cmin become the corner conditions for short interconnects.

G. Implementation in LPE

On implementation in LPE, each corner condition of all layers is combined to one cross-section. Therefore, there are four cross-sections of corner conditions. Then these four cross-sections and the center cross section are input to the RC library generator, and the RC parameters in the center condition and the ratio of RC parameters in each corner condition to those at the center condition is output to the RC library as coefficients. On a RC extraction for a design, the RC parameters are extracted at the center condition and those at the corner conditions are calculated by using the coefficients. Fig.11 shows the flow of the RC library generation along with the proposed method and TABLE II is the schematic view of the RC library.

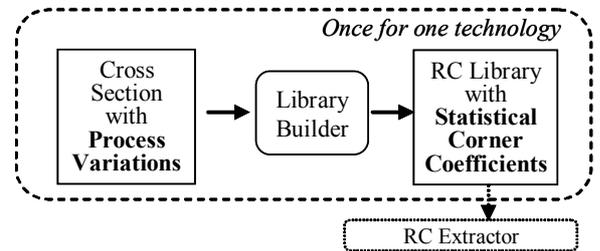


Fig. 11. Library Generator with Statistical Corner Conditions

TABLE II  
Schematic View of RC Library with Statistical Corner Coefficients

Patterns	Center Value		Corner Coefficients							
			RCmax		Cmax		RCmin		Cmin	
	R	C	$\beta_R$	$\beta_C$	$\beta_R$	$\beta_C$	$\beta_R$	$\beta_C$	$\beta_R$	$\beta_C$
1										
2	Center : R, C		Corner : $\beta_R \cdot R, \beta_C \cdot C$							
3										
...										

V. Statistical Corner Correction between Layers

The problem is that the variations of different interconnect layers are independent from each other because they come from different process steps. This means that the RC extraction from the cross-sections of corner conditions constructed by combining corner conditions of each layer would take into account situations that are statistically unlikely to happen, and would cause over-margins. The corner conditions can be brought even closer to the center condition by introducing statistical ideas to this problem.

Fig.12 shows the relation between the variations of two layers (M1 and M2) when an interconnect node is composed of these two layers. Fig.13 shows an extracted netlist with parasitic RCs involved with this node.

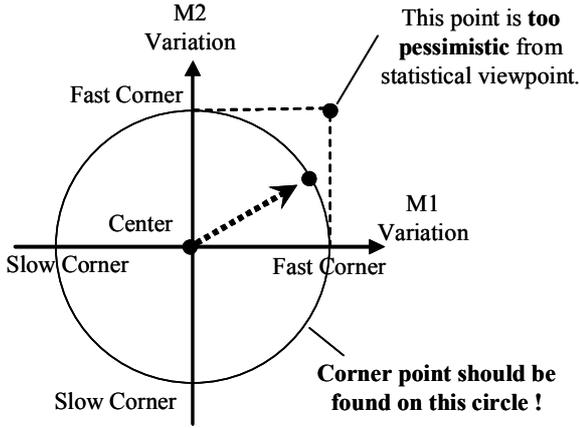


Fig. 12. Variation between Interconnect Layers

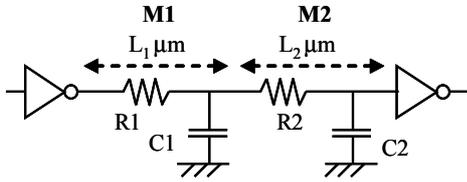


Fig. 13. Node composed of M1 and M2

A. Calculation of Statistical Corner Correction

The extracted R and C in one corner condition by the method proposed above (without statistical correction yet) can be expressed as “ coefficient( $\beta$ ) · center value(R or C) ”, shown in TABLE II. Note that only one R or C for one layer is described in Fig.13 for simplification but there can be many R or C (for each interconnect segment or pattern) actually, and the coefficients are also different.

Here, all these coefficients ( $\beta$ ) are changed to new coefficients ( $\beta'$ ) which is closer to 1 (= center condition) than  $\beta$  itself, by using  $\gamma$  shown in TABLE II, as follows;

$$\beta' = 1 + (\beta - 1) \cdot \gamma \quad (0 < \gamma \leq 1).$$

TABLE III  
Statistical Correction of Corner Coefficients

Center	Corner Condition without Statistical Correction	Corner Condition with Statistical Correction
R1	$\beta_{R1} \cdot R1$	$\beta_{R1}' \cdot R1$
C1	$\beta_{C1} \cdot C1$	$\beta_{C1}' \cdot C1$
R2	$\beta_{R2} \cdot R2$	$\beta_{R2}' \cdot R2$
C2	$\beta_{C2} \cdot C2$	$\beta_{C2}' \cdot C2$

$$\beta^{*'} = 1 + (\beta^* - 1) \cdot \gamma$$

B. Determination Method of Correction Coefficient

When the total length of M1 is  $L_1$  and that of M2 is  $L_2$  at this node as shown in Fig.13,  $\gamma$  is calculated as follows;

$$\gamma = (L_1^2 + L_2^2)^{1/2} / (L_1 + L_2).$$

The reason of this expression is explained as follows. This explanation is for capacitance but the same explanation can be applied to resistance. Two assumptions are set here.

Assumption 1) Capacitance for each unit length is constant for all patterns and layers. This capacitance value is temporarily called  $C_0$ .

Assumption 2) Coefficient of the corner condition ( $\beta$ ) is constant for all patterns and layers. This coefficient is temporarily called  $\beta_0$ .

Under these assumptions, the capacitance in the corner condition without correction is expressed by center value  $C_{total}$  as follows;

$$\beta_0 \cdot C_{total}$$

And the capacitance variations of each layer are expressed as follows;

$$\begin{aligned} \text{M1: } \Delta C_1 &= (\beta_0 - 1) \cdot C_0 \cdot L_1 \\ \text{M2: } \Delta C_2 &= (\beta_0 - 1) \cdot C_0 \cdot L_2 \end{aligned}$$

From a statistical viewpoint, using the independence of the variations between layers, the total capacitance variation is calculated as follows;

$$\begin{aligned} \Delta C_{total} &= C_{total} \cdot ((\Delta C_1/C_{total})^2 + (\Delta C_2/C_{total})^2)^{1/2} \\ &= C_{total} \cdot (\beta_0 - 1) \cdot \gamma. \end{aligned}$$

Therefore, the capacitance in the corner condition becomes;

$$C_{total} \cdot (1 + (\beta_0 - 1) \cdot \gamma) = \beta_0' \cdot C_{total}$$

It should be noted that an estimation error will be likely to grow when an actual interconnect does not satisfy these two assumptions. But these assumptions can be easily met for an interconnect node composed of long interconnect segments because they usually consist of various patterns or layers. A node that needs accuracy is usually a long one because it causes a large interconnect delay.

The similar calculation can be applied to nodes composed of more than two layers.  $\gamma$  is calculated as follows;

$$\gamma = (L_1^2 + L_2^2 + L_3^2 + \dots)^{1/2} / (L_1 + L_2 + L_3 + \dots)$$

For this corner correction, information of all nodes with interconnect length and layers is necessary. But LPE tools may need not to make this data because this can be output

from the “Routing and Placing” phase of design.

### C. Care for Branched Nodes

To extract resistances of a branched node, the calculation of  $\gamma$  for resistance becomes as follows. Resistances that contribute to a signal are limited to those on the path of the signal. Then, resistances should be limited to the path of the signal on  $\gamma$  calculation. As there would be plural  $\gamma$  for resistance of the root of nodes, maximum of these  $\gamma$  should be adopted.

On the other hand, all capacitance of a node contribute to a signal passing this node. Then, the calculation already shown doesn't need to be changed.

### D. Care for Coupling Capacitance

On coupling mode extraction,  $\gamma$  of a capacitance would be extracted from the both nodes to which this capacitance is connected, and these  $\gamma$  are generally different from each other. In these case, maximum of these two  $\gamma$  should be adopted.

Finally, the LPE flow becomes Fig.14, following Fig.12.

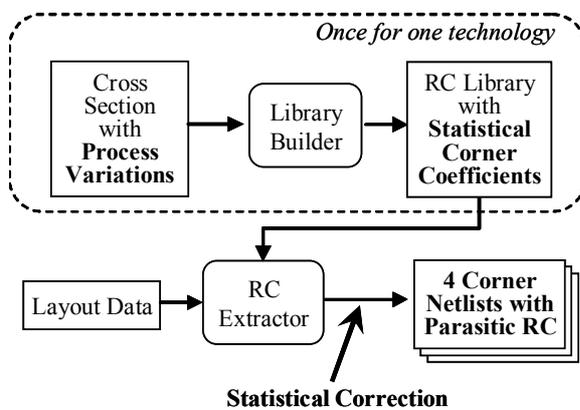


Fig. 14. LPE flow with Statistical Corner Conditions

## VI. Effects

By using the statistical corner conditions in a single layer, the guardband width from the fast corner to the slow corner decreases to a factor of  $1/(2^{1/2}) \approx 0.7$ , compared to that by conventional corner conditions. This factor of “0.7” is the ratio of the diameter of the circle and the diagonal of the square enclosing this circle in Fig.4. In other words, the corner conditions are brought closer to the center condition.

Moreover, the corner conditions are brought still closer to the center condition by using the statistical corner correction between layers. For example, suppose an interconnect node be composed of nine segments, all of which are different metal layers, but have the same length. In this case, the guardband width decreases to a factor of  $(9^{1/2})/9 \approx 0.33$  compared to that without the statistical corner correction. On the other hand, there is no effect to a node composed of a single layer. In average, the guardband width is 0.7 times of that without the corner correction.

With those two types of statistical aspects combined, the guardband width reduces to the half of the conventional one. Note both intralayer and interlayer reduction factors are 0.7, leading to an overall reduction factor of  $0.7 \cdot 0.7 \approx 0.5$ . In other words, if the capacitance or resistance variation range is +/-20% in the conventional corner conditions, it shrinks to +/-10% in the proposed statistical corner conditions. With narrower guardband, timing closure becomes easier. Narrower guardband allows designers the reduction of chip size and power consumption, and the full advantage of the present process technology in its performance.

## VII. Conclusions

Statistical ideas are introduced to the corner conditions for interconnect RC extraction. These ideas are utilized for trimming the over-margin caused by the conventional corner conditions. The basic idea is to exclude situations that are statistically unlikely to happen. By using two ideas, which are the statistical corner conditions in a single layer and the statistical corner correction between layers, the guardband width from the fast corner to the slow corner decreases by half, compared to that by the conventional corner conditions, in average. In other words, if the capacitance or resistance variation range is +/-20% in the conventional corner conditions, it shrinks to +/-10% in the proposed statistical corner conditions.

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