Equivalent circuit modeling of guard ring structures for evaluation of substrate crosstalk isolation

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Abstract— A substrate-coupling equivalent circuit can be derived for an arbitrary guard ring test structure by way of F-matrix computation. The derived netlist represents a unified impedance network among multiple sites on a chip surface and allows circuit simulation for evaluation of isolation effects provided by guard rings. Geometry dependency of guard ring effects attributes to layout patterns of a test structure, including such as area of a guard ring as well as location distance from the circuit to be isolated by the guard ring. In addition, structural dependency arises from vertical impurity concentrations such as p^+, n^+, and deep n-well, which are generally available in a deep-submicron CMOS technology. The proposed simulation based prototyping technique of guard ring structures can include all these dependences and thus can be strongly helpful to establish isolation strategy against substrate coupling in a given technology, in an early stage of SoC developments.

I. Introduction

Systems-on-a-chip (SoC) integrated circuits for mobile electronics often demands reconciliation of rich functionality and low cost, or even that of high performance and low power, where trends require to establish a successful design solution to incorporate CMOS RF front-end, baseband mixed-signal signal processing units, as well as application processors in a single die. Accurate prediction and reduction of substrate crosstalk have been technology challenges of quite importance in such CMOS mixed-signal/RF SoC designs [1]. Here, the substrate crosstalk is a phenomenon where noises injected by digital circuits into a common substrate propagate toward embedded analog circuits and leak to analog signal paths, which finally interfere with analog operation and degrade analog circuit performance.

Realization of chip-level substrate coupling analysis has been successfully achieved in several ways, where parasitic coupling in a silicon substrate is modeled as a lumped resistance [2][3], calculated from resistive network of meshed substrate media [4][5][6] or from integral of Green's function [7]. It should be noted that the models extracted by these techniques are represented in the form of a circuit description, for the purpose of simulating a circuit response including the substrate coupling. On the other hand, substrate-coupling reduction techniques have also been widely discussed, which include low-noise modification applied to CMOS digital logic cells [8] or layout/device level approaches [9][10]. Obviously, chip-level simulation is helpful to minimize substrate-coupling in a design, however, it is necessary to establish the way to model each substrate-coupling reduction techniques at layout and/or at circuit levels.

As is well known, the placement of guard bands in between circuits to be isolated among each other and/or guard rings surrounding substrate-noise sensitive devices must be a baseline measure to achieve isolation against substrate coupling, since this approach does not necessitate changes of a circuit design. Therefore, how large isolation can be achieved by a guard band/guard ring in a given technology should be evaluated at the initial stage of any SoC developments. This paper discusses a methodology to derive an equivalent circuit expression of a guard ring based on substrate coupling analysis using F-matrix computation in Section 2, and demonstrates evaluation of various guard ring structures in Section 3. A brief conclusion will be given in Section 4.

II. Substrate-coupling equivalent circuit

A. substrate-coupling in a CMOS technology

Representative substrate coupling paths parasitic to CMOS devices in a standard p-type bulk silicon technology include resistive connection of P-P-P and capacitive-resistive combined connections of N-P-P and N-N-P, as shown in Figure 1. Here, P-P-P couples arrays of substrate contacts at different locations, while N-P-P and N-N-P correspond to a capacitive coupling at source to bulk junction of N-channel MOSFET and well to bulk junction of P-channel MOSFET, respectively.

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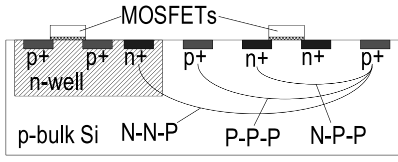

Fig. 1. Substrate coupling paths in CMOS technology.

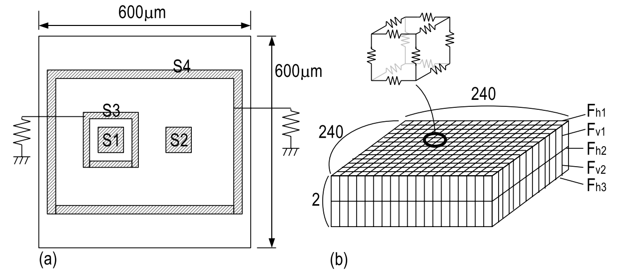

Fig. 2. (a) Test structure of substrate coupling, (b) meshing for extracting equivalent circuit.

B. F-matrix computation of substrate-coupling test structure

Figure 2(a) shows a test structure for evaluating substrate coupling, where two signal ports of S1 and S2, inner guard ring of S3 surrounding S1 port, and outer guard ring of S4 locate within the area of 600 μm × 600 μm. Here, isolation of S2 from S1 is measured as AC scattering parameter of S21. The effect of guard ring in reducing substrate coupling can be evaluated as the difference of S21 when S3 is connected to AC ground from that when S3 is floated. The outer guard ring (S4) is fixedly connected to the system ground in order to supply DC bias voltage of 0 V to the body of test structure formed on a p-type substrate. Here, a termination resistance of 50 Ω is inserted between S3 and AC ground as well as S4 and system ground, since isolation provided by guard-rings has to be effectively evaluated as is in an assembled chip.

A silicon substrate can be regarded as an equivalent resistive mesh, as long as the frequency of interest is within a few GHz. Therefore, we have applied 240 × 240 isotropic meshing to the test structure as shown in Figure 2(b), namely, mesh nodes are placed in every 2.5-μm distance in both x and y directions. In z direction, three layers with the same horizontal meshes are stacked with identical vertical separation. The resistivity of an individual mesh branch is determined from the impurity concentration at its position in a bulk.

In order to generate a compact equivalent circuit of the mesh stacks, mathematical preprocessing for network reduction such as [11] is necessary. We have applied a network reduction methodology using fundamental matrix (F-matrix) computation [12], where the test structure is dealt with as a resistive network in alternate piles of horizontal and vertical layers, as shown in Figure 2(b). Here, a multi-terminal F-matrix relates voltage V_2 and current I_2 of n output terminals to those of n input terminals V_1 and I_2 as follows:

$$\begin{bmatrix} \mathbf{V_1} \\ \mathbf{I_1} \end{bmatrix} = \mathbf{F} \begin{bmatrix} \mathbf{V_2} \\ \mathbf{I_2} \end{bmatrix}. \quad (1)$$

Cascading F-matrices gives a synthesized system F-matrix where all of the intermediate nodes are included to a single F-matrix, which is the most attractive feature of the F-matrix computation, as shown in the following equation.

$$\begin{bmatrix} \mathbf{V_{top}} \\ \mathbf{I_{top}} \end{bmatrix} = \mathbf{Fh_1 Fv_1 Fh_2 Fv_2 Fh_3} \begin{bmatrix} \mathbf{V_{btm}} \\ \mathbf{I_{btm}} \end{bmatrix}, \quad (2)$$

where (V_{top}, I_{top}) stand for the current and voltage of n nodes on the chip surface, (V_{btm}, I_{btm}) those on the chip bottom, $Fh_{1,2,3}$ and $Fv_{1,2}$ horizontal and vertical F-matrices within a substrate mesh, respectively. From the Kirchhof's laws, we can find $I_1 = I_2$ in determining vertical and $V_1 = V_2$ in determining horizontal F-matrices, respectively, and obtain general forms of F-matrices as follows:

$$\mathbf{Fv} = \begin{bmatrix} \mathbf{E} & \mathbf{A} \\ \mathbf{0} & \mathbf{E} \end{bmatrix}, \mathbf{Fh} = \begin{bmatrix} \mathbf{E} & \mathbf{0} \\ \mathbf{B} & \mathbf{E} \end{bmatrix}. \quad (3)$$

Here, A, B are sub-matrices representing vertical resistive elements determining vertical voltage differences and horizontal resistive elements determining horizontal currents induced from voltage differences from four neighboring nodes, respectively, and E an identity matrix. Although the synthesized system F-matrix relates (V, I) of all the surface nodes to those of the bottom nodes, we often represent a few of the nodes as explicit observation nodes and leave other nodes floated. Further network reduction can be performed in converting the F-matrix to a Y-matrix of the observation nodes under a condition where $I_{top-floated} = 0, I_{btm-floated} = 0$ for the other floated nodes. The final form of a substrate model is a SPICE compatible sub-circuit netlist, where the ports equivalent to the observation nodes are fully connected each other with resistors constituting the Y-matrix. Finally, three-dimensional test structure is well reduced to a two-dimensional equivalent circuit.

Figure 3 shows simulated frequency responses of S21 for P-P-P and N-P-P test structures. S1 port is covered with p^+ in P-P-P while with n^+ in N-P-P, on the other hand, S2 port and S3 guard ring surrounding S1 port are covered with p^+ in both structures. A lumped capacitor corresponding to junction capacitance of n^+ to p-type substrate in S1 port is estimated from cross-sectional

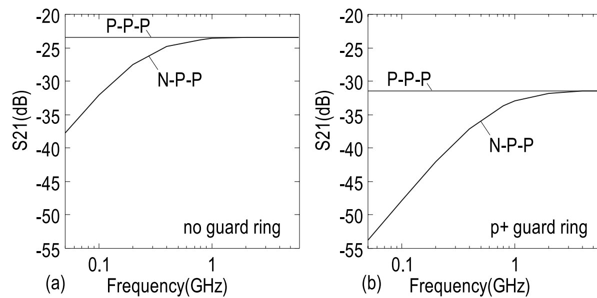

Fig. 3. Simulated S21 versus frequency dependence. Resistive (P-P-P) and capacitive (N-P-P) substrate coupling. (a)p+ guard ring (S3) is floated, (b) p+ guard ring (S3) is AC grounded.

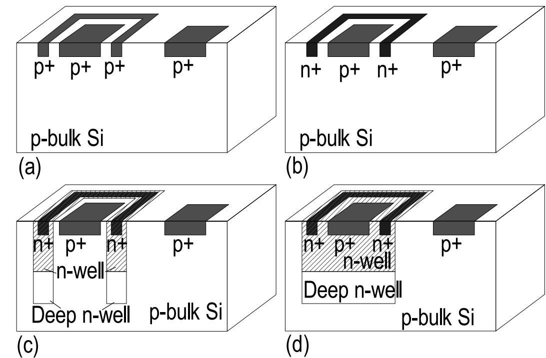

Fig. 4. Guard ring (GR) structures. (a) p^+ GR, (b) n^+ GR, (c) deep n-well GR, and (d) deep n-well pocket for comparison.

impurity profile and connected to a single observation node in S1 port of the computed N-P-P equivalent circuit. Here, the N-P-P test structure exhibits much higher isolation of S2 from S1 in low frequency range compared with the P-P-P counterpart, however, substrate coupling increases with 20 dB/decade against frequency due to capacitive coupling and finally dominated by frequency independent resistive coupling same as P-P-P for frequency higher than 2 GHz. It is also shown that the p^+-guard ring at S3 can effectively isolate S2 from S1 for substrate couplings in both structures, where the inclusion of guard ring structures in the test structure equivalent circuit will be detailed in the next section.

III. Evaluation of guard ring structure

A. Equivalent circuit modeling of guard ring structures

We have developed an enhanced F-matrix computation flow that can include various guard ring structures in an equivalent circuit of the test structure shown in Figure 4, where S1 port is covered with p^+ and surrounded by a guard ring or included in a deep n-well pocket, while S2 port is covered with p^+ and connected to a common p-type substrate. Here, a guard ring can be resistive such as p^+ or capacitive such as n^+ and deep n-well (DNW). While the former absorbs and drains out the currents flowing through a substrate, the latter inserts a high impedance cut on the current flow and forces to detour, both result in the increase of isolation between ports. Since these guard ring structures introduce impedance components that are sharply localized in space and also accompany exponential difference in magnitude from a bulk resistivity, F-matrix computation becomes almost impracticable because of very dense meshing in F-matrices and explosion of computation time as well as memory usage. In order to solve this issue and alleviate computation requirements, following two modifications are made to the basic F-matrix computation flow described in Section 2.

[Short or cut of observation points]

Since most of the area in the test structure of Figure 2(a) has identical vertical impurity profile, F-matrix computation accordingly to (2) is performed under the assumption of uniform impurity. Then, an equivalent circuit is derived from F-to-Y matrix conversion with observation points assigned along the periphery as well as within the surface of S1, S2, S3, and S4 areas as shown in Figure 5(a).

Here, we can assume that the observation points in each of S1, S2, S3, and S4 areas show identical node voltages when each of the area is entirely covered by a highly conductive sheet, roughly $10^3\times$ higher conductivity than the substrate, formed by selectively implanted high-density impurities and metal wirings. In this case, all the observation nodes within each of such areas are shorted together and provides a single representative port in a modified equivalent circuit as shown in Figure 5(b).

On the other hand, we can expect infinite isolation at DC from each of the S1, S2, S3, and S4 areas to the bulk when each of the area is entirely covered by junction capacitance against the bulk. In this case, the observation nodes within each of the areas are cut out and thus corresponding nodes are eliminated from a modified equivalent circuit, however, the observation nodes on the continuous periphery facing to the bulk are united to another single port as shown in Figure 5(c).

Note that mesh nodes other than the observation nodes are all included in the F-matrix computation to represent resistive networks in a bulk.

[Three level stacks of F-matrix cascade sub-models]

Impurity profile in a bulk-silicon CMOS technology shows strongly localized high concentration within a few μm depth from the surface and mostly constant low-level concentration in the rest of a bulk, typically with more than 500-μm thickness depending on assembly. In order

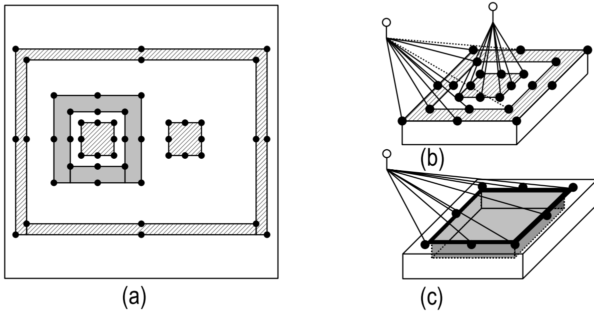

Fig. 5. (a) Assignments of observation points and providing (b) shorts or (c) cuts among observation points.

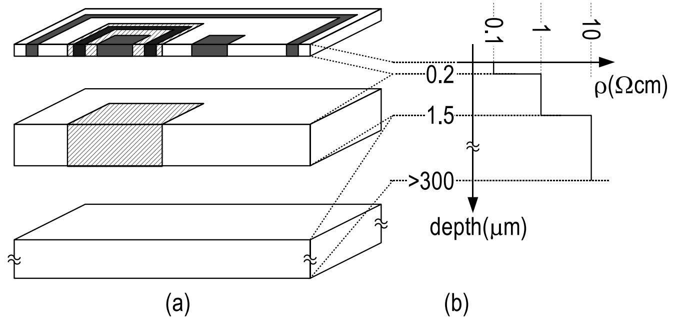

Fig. 6. (a) Stack of three F-matrix cascade sub-models corresponding to chip surface, well, and deep bulk, and (b) assumed impurity profile of guard ring test structure.

to include the surface impurity concentration properly in a full-depth F-matrix computation, we have divided the test structure vertically into three-level sub-models of chip surface, well, and deep bulk, as shown in Figure 6(a), where the chip surface sub-model has a depth identical to channel stop implant or p^+/n^+ active diffusions, the well sub-model has the depth corresponding to p-well or n-well, and the deep bulk sub-model covers the rest. Here, the areas of S1, S2, S3, and S4 defined in the layout of the surface sub-model are identically copied to the well and deep bulk sub-models for modeling purpose. Assumed vertical impurity is also shown in Figure 6(b).

A three-dimensional F-matrix cascade with the assumed uniform impurity concentration is built in each of the sub-models and then reduced to a two-dimensional equivalent circuit through F-matrix computation accordingly to (2) followed by F-to-Y matrix conversion with the short or cut of observation points in each of the S1, S2, S3, and S4 areas, as mentioned. The resultant sub-model equivalent circuit is described as a sub-circuit netlist with explicit ports relating to S1, S2, S3, and S4 areas. Finally, the entire test structure is modeled as a single equivalent circuit by stacking the three sub-models, namely, by connecting the explicit ports of the three sub-circuits, with intermediate lumped passive elements.

B. Evaluation of various guard ring structures

We have tailored the enhanced F-matrix computation flow so as to fit various guard ring structures and demonstrated that the three-level stacks of F-matrix cascade sub-models could successfully capture isolation characteristics. Here, all the p^+ guard ring structures are assumed to have p-well sub-models with uniform resistivity of 1 Ωcm and deep bulk sub-models with uniform bulk resistivity of 10 Ωcm as shown in Figure 6(b).

Figure 7 shows modeling of p^+ guard-ring test structure. The surface sub-model includes p^+ thus highly conductive areas of S1, S2, S3, and S4, where each of the areas can be united to a single port by shorting observation points, as was shown in Figure 5(b). The p-well and deep bulk sub-models also include S1, S2, S3, and S4 areas at the same position as the surface sub-model, and the areas each is similarly united to a corresponding single port in each sub-models. Finally, the three equivalent circuits are connected without intermediate elements (Figure 7(b)).

Figure 8 shows modeling of n^+ guard-ring test structure. The observation points within n^+ areas of S3 in the surface sub-model are cut out, as was shown in Figure 5(b). However, both inner and outer continuous peripheries of S3 area are united to each single port named $S3_{inner}$ and $S3_{outer}$, respectively. On the other hand, $S3_{top}$ is virtually re-defined as a single unified port corresponding to the eliminated n^+ area. In the well sub-model, S1, S2, S3, and S4 areas identically defined as the surface sub-model are filled with p-type dopant and thus each is united to a corresponding single port, where the S3 port is named $S3_{bottom}$. These ports relating to S3 area: $S3_{inner}$, $S3_{outer}$, and $S3_{bottom}$, are connected to $S3_{top}$ through lumped capacitors parasitic to peripheral junction C_{per} and bottom junction C_{btm}, in order to express the placement of n^+ guard ring in a final netlist (Figure 8(b)).

Figure 9 shows modeling of deep n-well guard-ring test structure. Although the modeling steps are same as in the n^+ guard-ring test structure, both of the surface and well sub-models are applied with the elimination of the observation points within S3 area and the creation of $S3_{inner}$ and $S3_{outer}$ in the peripheries of S3 area, since S3 area is deeply isolated from the other areas by the deep n-well guard ring. The re-definition of $S3_{top}$ is also performed in both sub-models, however, $S3_{bottom}$ is defined for S3 areas in the deep bulk sub-model. Again, the ports relating to S3 area are connected to $S3_{top}$ through lumped capacitors, in order to express the placement of deep n-well guard ring in a final netlist (Figure 9(b)).

Figure 10 shows modeling of deep n-well pocket test structure. In this case, the observation points within n^+

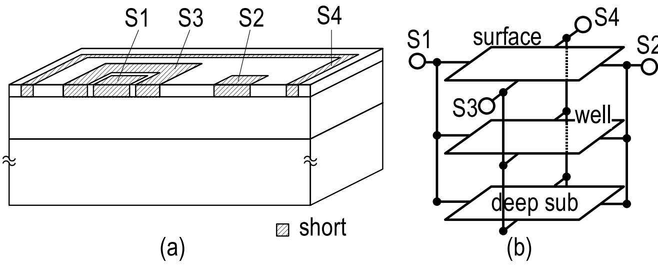

Fig. 7. (a) p^+ guard-ring test structure and (b) equivalent circuit.

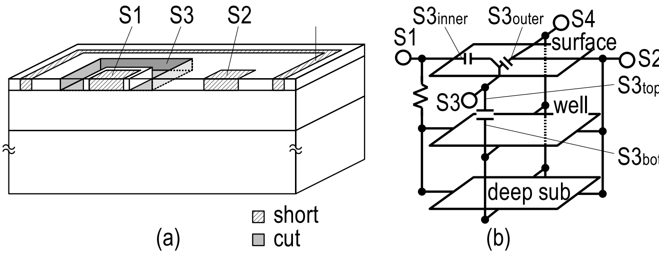

Fig. 8. (a) n^+ guard-ring test structure and (b) equivalent circuit.

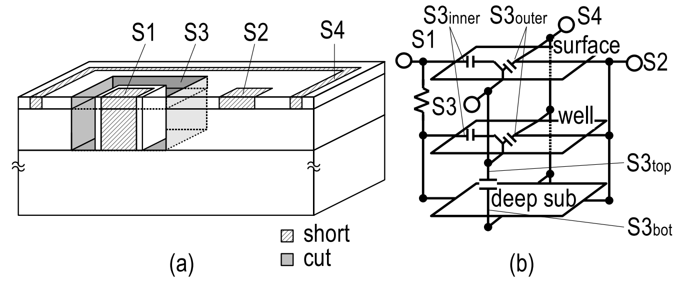

Fig. 9. (a) Deep n-well guard-ring test structure and (b) equivalent circuit.

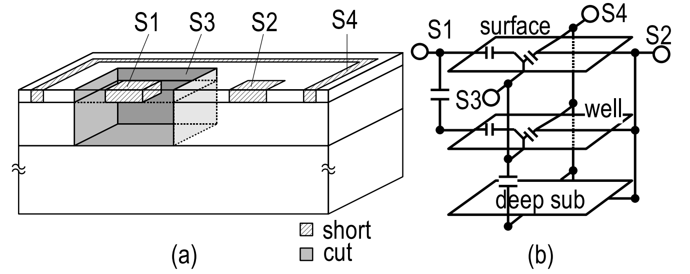

Fig. 10. (a) Deep n-well pocket test structure and (b) equivalent circuit.

areas of S3 in the surface sub-model are cut out, and moreover, those within the areas covered by a single deep n-well pocket in the well sub-model are also eliminated. On the other hand, the single port of $S3_{outer}$ is defined by shorting observation points along the periphery of the deep n-well pocket. The bottom plate is defined in the deep bulk sub-model as a single port of $S3_{bottom}$ covering the same footprint of the single deep n-well pocket.

Then, the re-defined S3 port of the single deep n-well is connected to S_3outer and $S3_{bottom}$ and also to the S1 port defined for S1 through lumped parasitic capacitors, in order to express the placement of deep n-well pocket in a final netlist (Figure 10(b)).

Figure 11 shows simulated and measured results of isolation effectiveness of p^+ guard ring with geometry dependency, where the models with different distance between S2 and S1 ports and those with various areas of S1 ports (and S3 guard rings as well) are evaluated. The measurement results of these structures shown in Figure 11 are reported in [13]. The results of simulation and measurement are well consistent.

Figure 12 compares isolation effectiveness achieved by various guard ring structures of p^+, n^+, and deep n-well, as well as by deep n-well pocket. It is as expected that p^+ guard ring provides moderate isolation within the entire frequency range. The most effective isolation for frequency beyond 1 GHz is achieved by deep n-well guard ring.

Figure 13 shows geometry dependence of isolation achieved by deep n-well guard ring and by deep n-well pocket, evaluated at 100 MHz for representing low frequency range as well as at 2 GHz for radio frequency (R-F) range. The superiority of the deep n-well guard ring in RF isolation is quite obvious, however, the effectiveness degrades due to capacitive couplings as S1 as well as S3 area enlarge. Here, the relatively small isolation in low frequency range can be supplemented by the combinational use with p^+ guard ring as is implied from Figure 11.

The derivation of test-structure equivalent circuits by the enhanced F-matrix computation flow took 30 minutes in average over various guard band structures, on a work station incorporating dual Ultra SPARC III running at 750 MHz and 2 GByte memory. In addition, a few minutes was required for S21 simulation by commercial SPICE circuit simulator.

IV. Conclusion

The proposed F-matrix computation flow realizes equivalent circuit modeling of various guard ring structures with geometry dependency as well as structural differences, by incorporating two novel techniques: three-level stacks of F-matrix cascade and short-or-cut of observation points. The isolation difference among p^+, n^+, and deep n-well guard rings is successfully evaluated along with distance as well as area dependencies. The combinational

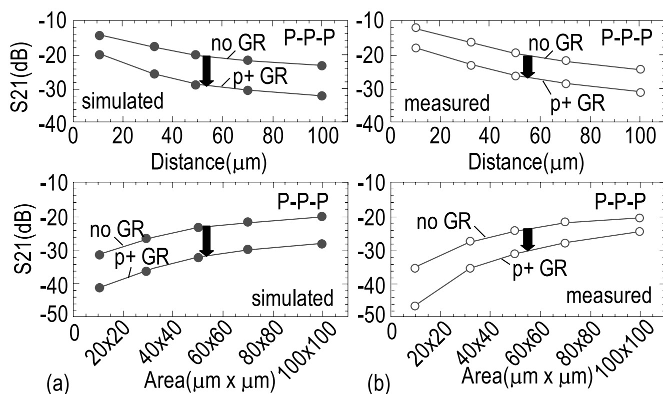

Fig. 11. (a) Simulated and (b) measured geometry dependency of GR isolation effects. The measurement results have been reported in [13].

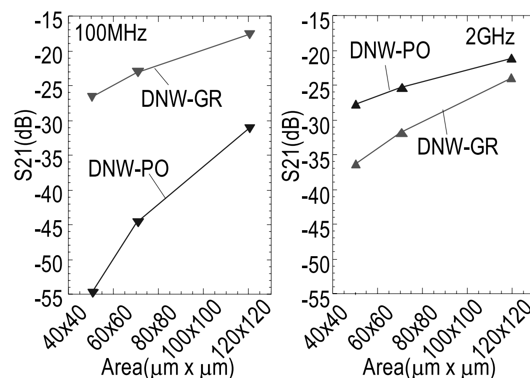

Fig. 13. Simulated geometry dependency of deep N-well guard ring (DNW-GR) and deep N-well pocket (DNW-PO).

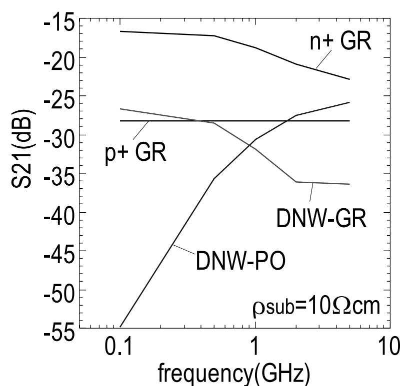

Fig. 12. Simulated S21 versus frequency dependence, comparing p^+-guard ring (GR), n^+-guard ring (GR), deep N-well guard ring (DNW-GR) and deep N-well pocket (DNW-PO). S1 and S2 has area of 50 μm × 50 μm.

use of p^+ and deep n-well guard rings are suggested by those simulations in terms of RF isolation. The proposed technique enables simulation based prototyping of guard ring structures, which can be strongly helpful to establish isolation strategy against substrate coupling in a given technology, in an early stage of SoC developments.

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