A Routability Constrained Scan Chain Ordering Technique for Test Power Reduction*

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Abstract— For scan-based testing, the high test power consumption may cause test power management problems, and the extra scan chain connections may cause routability degradation during the physical design stage. In this paper, a scan chain ordering technique for test power reduction under user-specified routability constraints is presented. The proposed technique allows the user to explicitly set the routing constraints and the achievable power reduction is rather insensitive to the routing constraints. The proposed method is applied to six industrial designs. The achievable power reduction is in the range of 37–48% without violating any user-specified routing constraint.

I. INTRODUCTION

The growing IC capacity and complexity have caused several manufacturing testing challenges one of which is the elevated power consumption during testing. Without careful test power management, the excess heat dissipation during testing may immediately damage the circuit under test (CUT) or cause reliability degradation problems.

It has been shown in [13] that the power in the test mode can be as much as twice that in the functional mode. The two major causes of the high test power consumption are:

Test pattern characteristics: ATPG and LFSR generated patterns are usually less correlated than functional patterns [12] and thus cause higher logic switching activities.

DfT circuitry operation: The scan flip-flops toggle at a higher rate during the scan chain shifting operations than in the normal mode. In [7], it is shown that, using traditional MUX-based scan flip-flops, the flip-flop short-circuit power alone already accounts for about 25% of the test power. As the IC capacity keeps growing, the situation will get worse due to the growing number of scan flip-flops.

Several approaches have been proposed to reduce test power consumption, and a detailed review is available in [9]. In general, the reported methods can be divided into the following categories: (1) power-aware test pattern generation (for external ATE or BIST), (2) test pattern and/or scan chain ordering, (3) primary input control to suppress logic transitions, and (4) scan chain and/or clock scheme modification to suppress logic transitions.

In this paper, we are interested in the scan chain ordering technique because it (1) has no negative impact on the test time and fault coverage, (2) impacts less on the design flow, and (3) can be easily combined with other power reduction techniques. In the past, when area and performance are the major design concerns, scan chain ordering techniques were proposed to reduce the total or average scan chain length [1, 6, 2, 10] so that routability and timing constraints are satisfied. However, as IC complexity multiplies, test power management has become the focus of recently reported scan chain ordering techniques.

In [8], a random ordering and a simulated annealing scan chain ordering algorithms are proposed for test power reduction. However, the proposed heuristics are not capable of handling large designs. Another simple yet efficient scan cell ordering method for test power reduction is reported in [5]. This technique first determines the scan cell chaining order to minimize scan cell transitions, and then identifies the input and output scan cells.

Routability-constrained test power reduction technique is reported in [3]. Based on the power reduction heuristic in [5], [3] divides the scan flip-flops into clusters. (An improved clustering method is proposed in [4].) By clustering, the inter-cell connections are limited to be within the clusters except for the inter-cluster connections that connect the scan chain segments of adjacent clusters into a single scan chain. One limitation, however, is the loose correlation between the clustering scheme and the commonly used routing constraints.

The main contribution of this paper is a scan chain ordering technique that reduces the scan chain test power under the user specified routing constraints. Compared to [3, 4], the advantages of our technique are as follows. First, the user can explicitly specifies the routing constraints, including the maximum distance between successive scan cells, and the total scan chain length. Secondly, the negative impact of routing constraints on power reduction is much less significant. Simulation results on six industrial designs are shown. Our technique achieves 37–48% test power reduction without violating any routing constraints. Furthermore, the power reduction performance is rather insensitive to the routing constraints.

The remaining of this paper is organized as follows. In Section II, we will briefly review the background and related researches. Details of the proposed technique is depicted in Section III. Experimental results on six industrial designs are presented in Section IV. Finally, we conclude this paper in Sec-

tion V.

II. PRELIMINARIES

The goal of scan chain ordering is to find a scan cell chaining order such that the power dissipation during the scan chain shifting operations is minimized. Since only the chaining order is modified, scan chain ordering techniques cause no negative impact on the fault coverage and test time, and can be integrated into current design flow more easily. One limitation of scan chain ordering techniques is that the generated scan chain order targets a fixed set of test patterns (and output responses). However, as IP reuse becomes common practice, this problem will diminish. Under the core-based design methodology, the IP users' responsibility is to integrate the individual IP's test plan, and it is the IP designer that determines which test vectors, whether from external ATE or on-chip LFSR, to apply to achieve the specified fault coverage.

In the following, we will briefly review the background and related research on scan chain ordering.

A. Power dissipation definitions

Among the several definitions of test power consumption, e.g., total power (energy), average power, instantaneous power, peak power, the proposed technique concerns the total power and the peak power. Total power consumption is the sum of power during test application, and peak power is the highest value of power at any given instant.

B. Power dissipation of scan-based testing

Power dissipation during scan shifting can be divided into two parts: the scan cell switching activities and the induced logic switching activities. In practice, exact evaluation of the total switching activities during shift operations is time consuming. In [11], it is shown that the number of scan chain transitions and the induced logic element transitions are fairly closely correlated. Thus, the number scan chain switching activities is a good indication of the overall power consumption during scan chain shift operations.

C. Weighted scan chain transition [11]

For convenience, we will first list the notations used throughout the rest of the paper.

$c_1, c_2, \ldots, c_f$: The f scan cells in the circuit under test.

$O = (o_1, o_2, \ldots, o_f)$: A scan chain order that contains the f scan cells with the scan-in port at the first position. o_i's must be such that $o_i \in \{1, 2, \ldots, f\}$ and $o_i \neq o_j$ if $i \neq j$. For example, $O = (2, 5, 3, \cdots, 7)$ corresponds to the following scan chain configuration:

scan in $\rightarrow c_2 \rightarrow c_5 \rightarrow c_3 \cdots \rightarrow c_7 \rightarrow$ scan out

$V = (v_1, v_2, \ldots, v_f)$: An f-bit test pattern, where bit v_i is to be shifted to cell c_i for test application. For a given scan chain order $O = (o_1, o_2, \ldots, o_f)$, V is scanned in in the order $\left(v_{o_f}, v_{o_{f-1}}, \cdots, v_{o_2}, v_{o_1}\right)$—$v_{o_f}$ first.

$R = (r_1, r_2, \ldots, r_f)$: An f-bit test response, where bit r_i is the test response captured at cell c_i. R is scanned out in the order $\left(r_{o_f}, r_{o_{f-1}}, \cdots, r_{o_2}, r_{o_1}\right)$—$r_{o_f}$ first.

The weighted transition of a test pattern V, denoted by $WT(V)$ is defined as

$$WT(V) = \sum_{i=1}^{f-1} i \cdot \left(v_{o_i} \oplus v_{o_{i+1}}\right) \quad (1)$$

In this equation, the $\oplus$ operator detects if a transition exists between two successive scan-in values v_{o_i} and $v_{o_{i+1}}$. (We associate the two output values, *true* and *false*, of the $\oplus$ operator with the two numerical values, 1 and 0, respectively.) It can be easily shown that a transition between v_{o_i} and $v_{o_{i+1}}$, if exists, will cause a total of i scan cell state transitions. i is thus referred to as the weight of the transition between v_{o_i} and $v_{o_{i+1}}$.

For a set of m test vectors, $V^1, V^2, \ldots, V^m$, the number of total weighted transitions is

$$WT\left(\{V^1, V^2, \ldots, V^m\}\right) = \sum_{j=1}^{m} \sum_{i=1}^{f-1} i \cdot \left(v_{o_i}^j \oplus v_{o_{i+1}}^j\right) \quad (2)$$

where $v_{o_i}^j$ is the o_i-th bit of the vector V^j. Similarly, the number of weighted transitions associated with a set of m output responses, $R^1, R^2, \ldots, R^m$, where $R^i = \left(r_1^i, r_2^i, \ldots, r_f^i\right)$, is

$$WT\left(\{R^1, R^2, \ldots, R^m\}\right) = \sum_{j=1}^{m} \sum_{i=1}^{f-1} (f-i) \cdot \left(r_{o_i}^j \oplus r_{o_{i+1}}^j\right) \quad (3)$$

The only difference between Eq. 2 and Eq. 3 is the transition weight assignment, which reflects the fact that one is scanned into and the other is scanned out of the chain.

Consider the example in Fig. 1(a) in which $O = (1, 2, 3, 4)$, $V = (1011)$, and $R = (0101)$. For the test vector V, there are two transitions whose weights are 1 and 2, respectively. Thus, $WT(V) = 1 + 2 = 3$. Similarly, for the output response R, there are three transitions and $WT(R) = 3 + 2 + 1 = 6$. In Fig. 1(b), the scan chain order is modified to $O = (2, 4, 3, 1)$, and the weighted transitions are reduced to $WT(V) = 1$ and $WT(R) = 2$, which corresponds to a 66% reduction.

D. Past related works

In [3], routing constrained scan chain ordering for power reduction is investigated. The reported technique consists of three steps: (1) dividing scan cells into clusters according to their locations, (2) preforming scan chain ordering within each cluster to reduce test power, and (3) connecting adjacent clusters according to a pre-determined order. Because routing constraints are enforced by clustering, this approach has the following limitations:

Degraded power reduction: Clustering substantially sacrifices the achievable power reduction because most of the scan flip-flops are connected based on the closest neighbor criteria and only a few of them are connected according to test power optimization. In [4], the clustering method is modified for more evenly distributed scan flip-flops per cluster. Although the
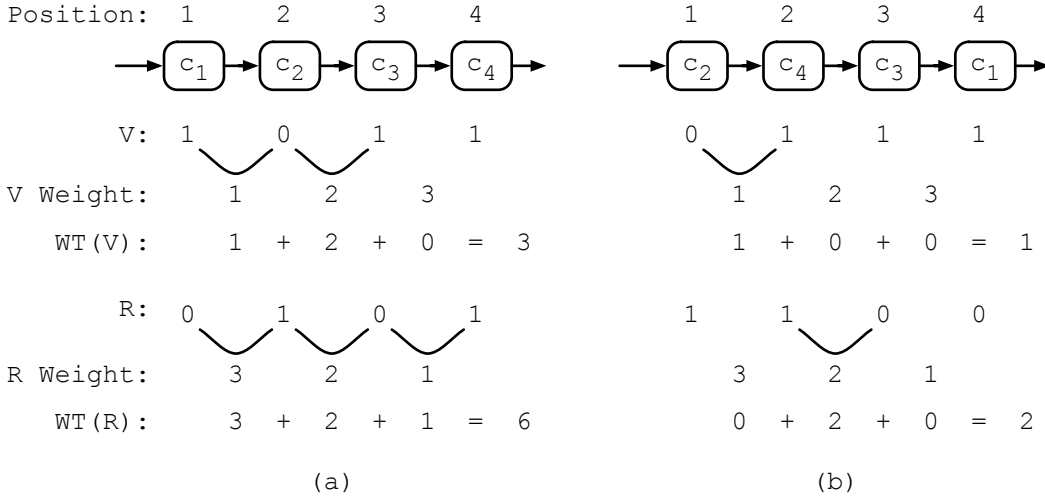
Position: 1 2 3 4   1 2 3 4

Fig. 1. Weighted transition.

achievable power reduction is improved by 3%, the above mentioned limitation still exists.

Difficulties in determining the clustering schemes: It is nontrivial to determine how the clusters should be formed to satisfy the desired routing constraints, e.g., the maximum distance between successive scan cells and the total scan chain length. The designer may have to try several different clustering schemes before the routing constraints are satisfied.

III. THE PROPOSED TECHNIQUE

In this paper, we propose a novel scan cell ordering technique that minimizes the shift operation power dissipation while satisfying the given routing constraints. The proposed algorithm is shown in Algorithm 1. Its inputs consist of

Test information: The sets of test vectors and responses.

FF information: The position (x_i, y_i) and power consumption factor p_i of each scan cell c_i. The reason to consider the individual flip-flop power consumption is to reflect the fact that the power consumption of each cell is affected by its size and load.

Routing constraints: The routing constraints include L_{max}, the maximum allowable scan chain length, and l_{max}, the maximum allowable Manhattan distance between two successive scan cells.

The output of the algorithm is the scan chain order O.

A. The algorithm flow

At the beginning of the algorithm, the routability bias factor β is set to zero and the initial order O is empty (lines 1–2). Setting β to zero causes the routing constraints to be ignored. Then, the cost graph G is constructed (line 3). In G, there is a vertex corresponding to each scan cell, and there is an undirected edge between a pair of scan cells if the Manhattan distance between the two cells is less than l_{max}. Each edge is associated with the power consumption and routability information of the cells it is connected to. In line 4, the first scan cell, i.e., the scan-in port, is selected. Choice of this first cell is

application dependent. It may be selected randomly if no constraint is given, or be such that the resulting weighted transition is further minimized (as in [5, 3, 4]). Here, we choose the one closest to the assigned scan in pin location as the first scan cell. The selected SI cell then becomes the current flip-flop, CF, and is appended to O (line 5).

From line 6 to 20 is the main ordering algorithm which terminates when all the scan cells are connected without violating any routing constraint. Each time, the next scan cell NF is selected using a greedy search heuristic (line 7). Note that the greedy heuristic may not return any next cell (line 8) if CF is not connected to any un-ordered scan cell due to the l_{max} constraint. For such cases, the algorithm will abandon the current results, adjust the routability bias factor β, empty O, and then start a new iteration (lines 9–11). After appending NF to O and making it CF, the L_{max} constraint is examined (line 15). In case of L_{max} violation, the same procedure as l_{max} violation is taken (lines 16–18).

B. Constructing the cost graph

As shown in Algorithm 1, our scan chain ordering heuristic relies on the cost graph to greedily add scan cells to the scan chain. The three steps to construct the cost graph G are:

1. For each scan cell c_i, add a vertex n_i to G.

2. For each pair of scan cells (c_i, c_j), $i \neq j$, add an edge e_{ij} between (n_i, n_j) if the Manhattan distance D_{ij} between c_i and c_j, defined as

$$D_{ij} = |x_i - x_j| + |y_i - y_j|$$

is less than l_{max}.

3. Associate with each edge e_{ij} the transition frequency T_{ij} and Manhattan distance D_{ij} between c_i and c_j. To obtain the transition frequency T_{ij}, a vector B_i is first derived. B_i consists of the test vector bits to appear and the response bits to be captured in c_i, i.e., $B_i =$

```
Test Information    :
        Test vectors V¹, V², ..., Vᵐ
        Test responses R¹, R², ..., Rᵐ
FF Information      :
        FF locations (xᵢ, yᵢ)
        FF power consumption factor pᵢ
Routing Constraints:
        Maximum successive scan cell distance l_max
        Maximum total scan chain length L_max

Output              :
        Scan chain order O

 1  β ← 0;
 2  O ← φ;
 3  G ← constructCostGraph();
 4  CF ← identifySI();
 5  append(CF, O);
 6  while size(O) < f do
 7      NF ← greedyNext(CF,O,G);
 8      if NF == null then
 9          β ← adjustBias();
10          O ← φ;
11          goto 4;
12      end
13      append(NF, O);
14      CF ← NF;
15      if chainLength(O) > L_max then
16          β ← adjustBias();
17          O ← φ;
18          goto 4;
19      end
20  end
21  return O ;
```

Algorithm 1: The proposed algorithm

$\left(v_i^1, r_i^1, v_i^2, r_i^2, \ldots, v_i^m, r_i^m\right)$ where m is the number of test vectors. T_{ij} is then defined as

$$T_{ij} = \frac{H\left(B_i, B_j\right)}{2 \cdot m}$$

where H denotes Hamming distance.

C. Finding next scan cell

In our algorithm, the greedyNext() function determines the next scan cell to be appended to the scan chain. First, the scan cells that are adjacent to CF and not ordered are identified and form the candidate set. Let c_i be the current flip-flop CF. For each cell c_j in the candidate set, the cost of appending c_j to the scan chain is defined as

$$cost\left(i, j\right) = \alpha \cdot T_{ij} \cdot p_j/p_{max} + \beta \cdot D_{ij}/l_{max} \quad (4)$$

where p_{max} is the maximum power consumption factor, α is set to 100, and β is automatically adjusted by the algorithm. Once all the costs are available, the lowest cost scan cell is selected as the next cell NF.

D. Bias adjustment

In the cost function (Eq. 4), one can adjust the two scaling factors α and β to control the bias of the scan chain ordering towards power reduction or routability. Since the goal is to optimize power consumption, in our algorithm, α is fixed at 100. The initial value of β is set to zero at the beginning and incremented by one each time any of the routing constraints is violated and thus the adjustBias() function is called. The underlying idea of this strategy is to ignore the routing constraints unless necessary so that we can arrive at better power reduction.

E. Extension to multiple scan chains

The proposed algorithm can also be applied to multiple scan chain designs. First, we can group the scan cells that belong to the same clock domain and/or the same sub-circuit into clusters. Then, the proposed technique is applied to each cluster for test power reduction.

IV. EXPERIMENTAL RESULTS

To validate our idea, we use a set of six industrial designs to perform various experiments. Each of the test cases comes with an initial scan chain ordering. Statistics of the designs are shown in Table I. The number of scan cells of each design is listed in column two. It ranges from 596 to 53,946. In columns three and four, the x and y spans correspond to the width and height of the smallest rectangle that encloses all the flip flops. In column five, the maximum allowable successive scan cell distance l_{max} is listed. The other routing constraint, maximum allowable scan chain length L_{max}, is listed in column six. Not shown in the table, the position and power consumption factor of each flip-flop are also provided.

TABLE I
CIRCUIT STATISTICS

design	# cell	x span	y span	l_{max}	L_{max}
1	596	643	1,252	648	147,124
2	596	990	1,188	748	130,269
3	8,755	2,810	2,338	1,146	1,745,662
4	6,389	3,781	1,261	1,536	4,158,421
5	5,994	1,670	1,774	1,016	1,571,524
6	53,946	5,670	5,774	2,693	22,638,289

The proposed technique is applied to the six designs and the experimental results are shown in Table II. In the total power column, the optimized test power and the improvement compared to the original ordering are shown. The power reduction is in the range of 37–48%. In the peak power column, the peak power of the optimized scan chain and the improvement are shown. Peak power reduction is in the range of 10–22%. In the l column, the maximum successive scan cell distances of the optimized scan chains are shown. Not only the constraint is satisfied, but also the maximum lengths are substantially reduced. In the L column, the scan chain lengths of the optimized scan chains are listed. Again, our algorithm actually

TABLE II
EXPERIMENTAL RESULTS

design	Total power optimized	gain (%)	Peak power optimized	gain (%)	l optimized	gain (%)	L optimized	gain (%)	β	CPU (sec)
1	16.64e06	37.99	597	11.94	643	60.98	95,341	65.77	11	2
2	15.02e06	39.57	567	10.88	740	60.99	129,553	54.34	9	2
3	3.04e09	43.69	7,201	16.37	1,060	72.06	1,398,054	89.17	12	368
4	1.59e09	44.69	5,308	15.20	1,536	67.63	1,553,632	85.05	11	229
5	1.43e09	44.08	5,041	15.14	969	65.31	967,173	75.38	12	280
6	71.33e09	48.19	40,455	22.09	2,456	77.20	12,190,595	94.21	23	16,005

significantly reduces the total length. The last two columns are the final β values and the CPU times, respectively.

To investigate the effect of routing constraints on the power reduction performance, we perform further experiments on the second design. In the first experiment, we vary l_{max} from 2,000 to 400 with L_{max} fixed at 240,000 and the results are shown in Table III. In columns two and three, the total and peak power reduction percentages are shown. No apparent degradation is observed until l_{max} is reduced to 400, a rather stringent constraint. On the other hand, columns four and five show that both l and L are reduced as l_{max} decreases.

TABLE III
IMPACT OF l_{max} CONSTRAINT ON POWER REDUCTION PERFORMANCE

l_{max}	Gain Total(%)	Peak (%)	Gain l (%)	L (%)	β
2,000	41.85	13.93	6.59	16.42	7
1,600	41.69	13.67	16.34	23.60	6
1,200	41.44	10.06	37.06	30.77	6
800	41.35	12.62	57.83	21.12	2
400	34.18	6.58	79.70	77.66	24

In the second experiment, l_{max} is fixed at 800 while L_{max} is gradually decreased from 240,000 to 80,000. The results are shown in Table IV. The same trend as Table III is observed.

TABLE IV
IMPACT OF L_{max} CONSTRAINT ON POWER REDUCTION PERFORMANCE

L_{max}	Gain Total(%)	Peak (%)	Gain l (%)	L (%)	β
240,000	41.35	12.62	57.83	21.18	2
200,000	40.91	7.29	58.14	34.32	4
160,000	39.56	10.70	58.14	54.07	9
120,000	39.00	10.55	58.14	57.82	11
80,000	36.22	6.86	60.57	71.94	28

V. CONCLUSION

In this paper, a novel routability constrained scan chain ordering technique for test power reduction is proposed. Simulation results on six industrial designs show significant power reduction. Furthermore, the algorithm is rather insensitive to routing constraints. Our future work will be to get more accurate power consumption information using commercial tools.

REFERENCES

[1] S. Barbagallo, M. L. Bodoni, D. Medina, F. Corno, P. Prinetto, and M. S. Reorda. Scan insertion criteria for low design impact. In *VLSI Test Symposium*, pages 26–31, 1996.

[2] S. Barbagallo, G. Borgonovo, D. Grassi, D. Medina, F. Corno, P. Prinetto, and M. S. Reorda. Scan chain partitioning and reordering based on layout information: an industrial experience. In *Design, Automation and Test in Europe*, 1998.

[3] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch. Efficient scan chain design for power minimization during scan testing under routing constraint. In *International Test Conference*, pages 488–493, 2003.

[4] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, and A. Virazel. Design of routing-constrained low power scan chains. In *Design, Automation and Test in Europe*, pages 16–20, 2004.

[5] Y. Bonhomme, P. Girard, C. Landrault, and S. Pravossoudovitch. Power driven chaining of flip-flops in scan architectures. In *International Test Conference*, pages 796–803, 2002.

[6] C. S. Chen, K. H. Lin, and T. T. Hwang. Layout driven selection and chaining of partial scan flip-flops. In *Design Automation Conference*, pages 262–267, 1996.

[7] M.-H. Chiu and J. C.-M. Li. Jump Scan: A DFT technique for low power testing. In *VLSI Test Symposium*, pages 277–282, 2005.

[8] V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. Reddy. Techniques for reducing power dissipation during test application in full scan circuits. *IEEE Transactions on CAD*, 17(12):1325–1333, December 1998.

[9] P. Girard. Survey of low-power testing of VLSI circuits. *IEEE Design & Test of Computers*, 19(3):82–92, May–June 2002.

[10] M. Hirech, J. Beausang, and X. GU. A new approach to scan chain reordering using physical design information. In *International Test Conference*, pages 348–355, 1998.

[11] R. Sankaralingam, R. R. Oruganti, and N. A. Touba. Static compaction techniques to control scan vector power dissipation. In *VLSI Test Symposium*, pages 35–40, 2000.

[12] S. Wang and S. K. Gupta. DS-LFSR: A new BIST TPG for low heat dissipation. In *International Test Conference*, pages 848–857, 1997.

[13] Y. Zorian. A distributed BIST control scheme for complex VLSI design. In *VLSI Test Symposium*, pages 4–9, 1993.