

# Analysis and Optimization of Gate Leakage Current of Power Gating Circuits\*

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**Abstract**— Power gating is widely accepted as an efficient way to suppress subthreshold leakage current. Yet, it suffers from gate leakage current, which grows very fast with scaling down of gate oxide. We try to understand the sources of leakage current in power gating circuits and show that input MOSFETs play a crucial role in determining total gate leakage current. It is also shown that the choice of a current switch in terms of polarity, threshold voltage, and size has a significant impact on total leakage current. From the observation of the importance of input MOSFETs, we propose the power optimization of power gating circuits through input control.

## I. INTRODUCTION

With CMOS technology scaling, subthreshold leakage current experiences an exponential growth mainly due to the scaling down of the threshold voltage. Many circuit level approaches have been proposed including dual threshold CMOS [1], variable threshold CMOS [2], input vector control [3], power gating [4], and so on. Power gating is shown to be especially efficient and conceived as a main circuit technique by many semiconductor companies [5], [6].

Power gating is realized by using a current switch, which can be either nMOSFET (footer) or pMOSFET (header), as shown in Fig. 1. When the power management unit (not shown in Fig. 1) detects the sufficiently long period of idle time, a sleep signal is applied to the gate of the current switch to disconnect  $V_{dd}$  or ground from a logic block. When it detects the logic block to be requested, the sleep signal is de-asserted to connect the logic block to the power rail. The logic block usually employs low  $V_t$  to sustain its performance, while high  $V_t$  is used for the current switch to suppress its subthreshold leakage current. Nevertheless, the same low  $V_t$  can be used for the current switch with the advantage of using single  $V_t$  on a chip and of using the switch of smaller size, but at the cost of increased subthreshold leakage current [5].

While being efficient to suppress subthreshold leakage current, power gating circuits suffer from *gate leakage current*, which grows very fast with scaling down of gate ox-

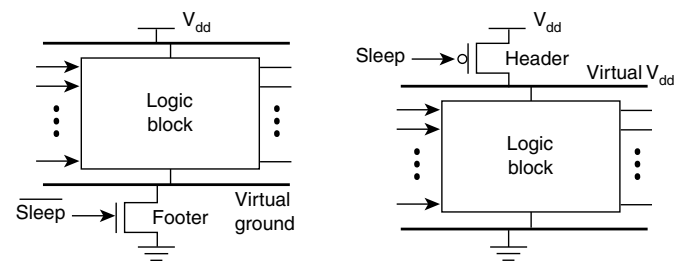


Fig. 1. Power gating circuits.

ide. In fact, gate leakage current is expected to exceed subthreshold leakage current when channel length is reduced to 60nm [7]. There are two kinds of gate leakage current depending on the bias condition of MOSFET: forward biased one and reverse biased one [8]. The former mainly consists of gate-to-channel tunneling current, which flows from gate to source/drain through channel. The latter is mainly composed of edge-direct-tunneling current, which flows from source/drain to gate through source-drain extension. The reverse biased gate leakage current is less than the forward biased one: e.g. about 30% less in our experiment with 45nm predictive technology model [9] [10] when the source and drain voltage levels are equal, and the gate has opposite voltage level.

Once in sleep mode, i.e. the current switch is turned off, the drain voltage of the current switch becomes close to either  $V_{dd}$  (footer) or ground (header). Since all internal node voltages of the logic block are close to  $V_{dd}$  or ground as well, the overall leakage current is determined by subthreshold and gate leakage current of the current switch [11]. Gate leakage current is dominant when high  $V_t$  is used for the current switch to suppress its own subthreshold leakage current. Since gate leakage current of pMOSFET is an order of magnitude smaller than that of nMOSFET, header is preferred in view of total leakage current [11].

However, this is not true in practice, since the primary inputs of most power gating circuits maintain their logic states even when sleep. This is because logic blocks that drive them may

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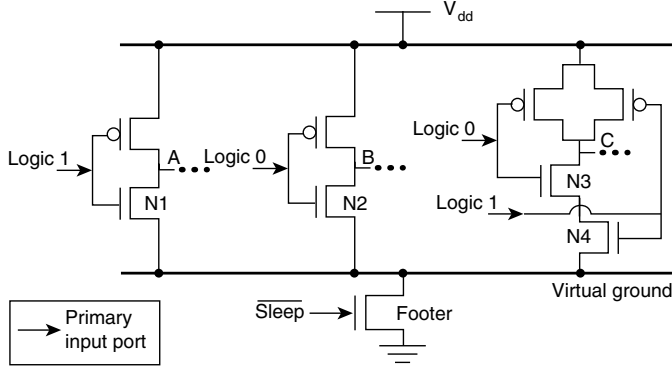


Fig. 2. Power gating circuit with a footer.

not exploit power gating (thus, always maintain logic) or may be in active. Since the sources and drains of the input transistors, which are internal nodes of the logic block, are biased to potential close to either  $V_{dd}$  or ground, there are reverse biased or forward biased gate leakage current depending on the bias condition of gate inputs.

In this paper, we study the sources of leakage current in power gating circuits and show that the input transistors play a crucial role in determining overall leakage current. It is also shown the choice of a current switch in terms of  $V_t$  voltage and size for optimization of total leakage current of a power gating circuit in idle state. From the observation of the importance of the input transistors, we propose the power optimization of power gating circuits through input control.

The remainder of the paper is organized as follows. In the next section, we study the sources of leakage current in power gating circuits, and address the problem of current switch design. In section III, we present power optimization of power gating circuits through input control and draw conclusions in section IV.

## II. GATE LEAKAGE CURRENT AND CURRENT SWITCH DESIGN OF POWER GATING CIRCUITS

### A. Mechanism of Gate Leakage Current in Power Gating Circuits

Fig. 2 shows a power gating circuit with a footer. When the circuit is in active (the footer is turned on), the voltage of virtual ground is close to ground, which is determined by the size of the footer and the current that flows into the footer. Once in sleep (the footer is turned off), virtual ground slowly goes up until it reaches a steady state potential, which is close to  $V_{dd}$ . The steady state potential and the time it takes to reach are determined by the amount of current flows in the logic block and in the footer. Fig. 3 shows how virtual ground reaches a steady state for one of ISCAS benchmark circuit, called C5315. It takes 82ns ( $t_1 - 5$ ) after the footer is turned off for virtual ground to reach 90% of the steady state ( $t_2$ ) voltage of 876mV, which is 24mV less than  $V_{dd}$ .

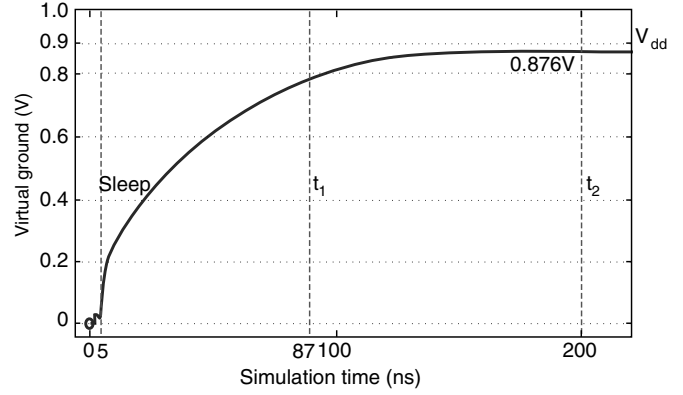


Fig. 3. The trace of virtual ground with a footer turned-off.

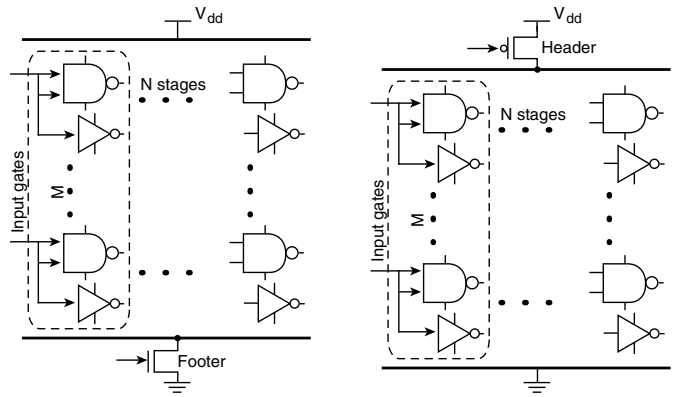


Fig. 4. Simulation circuits for measuring input gate leakage current.

Once in steady state, the footer induces reverse biased gate leakage current due to its bias condition. Also, nMOSFETs connected with primary inputs are another sources of gate leakage current (input gate leakage current). Assuming that the primary inputs are driven by logic blocks that are in active, N2 induces large reverse biased gate leakage current (70% of forward biased one) due to the large voltage difference between its gate and source/drain. Note that reverse biased gate leakage current of pMOSFET is negligible. N1 induces gate leakage current as well, but it is negligible compared to that of N2, since the voltage difference between the gate and source/drain is small. In the case of nMOSFET stack (N3 and N4), N3 induces reverse biased gate leakage current while the gate leakage current in N4 is negligible.

### B. Impact of Input Gate Leakage Current

The impact of input gate leakage current is determined by the number of transistors that are connected to primary inputs. Fig. 4 shows the simulation circuits to study the influence of input transistors on total leakage currents. The logic block consists of two types of gate chains: inverter chain and 2-input nand chain.<sup>1</sup> We vary the number of each type of gate chains, denoted as  $M$ , and the number of stages of gate chains, denoted

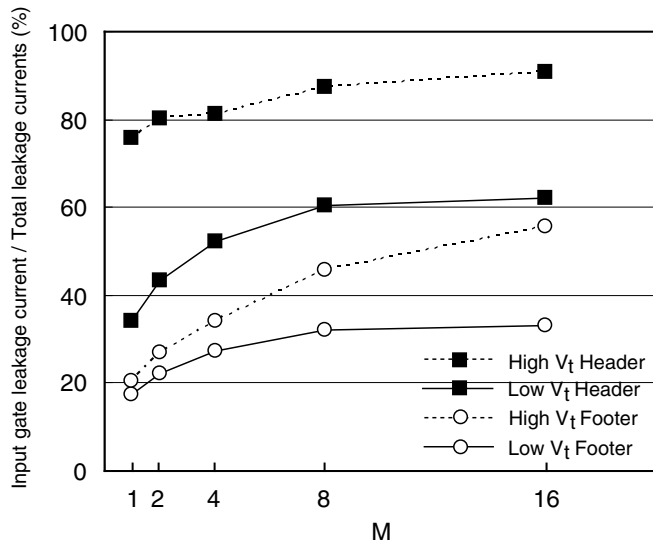


Fig. 5. Input gate leakage current ( $T=27^{\circ}\text{C}$ , low  $V_t = 220\text{mV}$ , high  $V_t = 400\text{mV}$ ).

as  $N$ , while keeping the number of inverters and nand gates to 48 respectively (i.e. there are  $M$ -inverter chains and  $M$ -nand chains with each chain consisting of  $N$  gates while keeping  $M \times N = 48$ ). We assign logic 0 to all primary inputs when a footer is used as a current switch, since it maximizes input gate leakage current (recall the previous subsection). Similarly we assign logic 1 to all primary inputs in the case of a header. The size of the switch is determined such that the delay of the logic block increases less than 3% compared to non-power-gated circuit.

Fig. 5 is the simulation result with 45nm predictive technology model, and shows that input gate leakage current can be a large portion of total leakage currents when power gating circuits are in sleep. As an example, input gate leakage current is about 34% of total leakage currents when a high  $V_t$  footer is used and the input transistors are  $8.3\%^2$  ( $M = 4$ ) of total transistors. This goes up to 45% when the input transistors get twice ( $M = 8$ ). When we use low  $V_t$  for a footer (e.g. when dual  $V_t$  is not available or when we want to reduce the size of a footer while keeping the same performance), subthreshold leakage current increases substantially due to its exponential dependency on threshold voltage. This increases the total leakage currents, while input gate leakage current remains almost constant. Thus, the portion of input gate leakage current gets smaller as is evident in Fig. 5. If we use a header instead of a footer, input gate leakage current is even more important since gate leakage current of a pMOSFET switch (header) is an order of magnitude lower than that of an nMOSFET switch (footer).

<sup>1</sup>Gate leakage current is different for different types of gates, and we use inverter and 2-input nand gate to reflect gate-wise variation.

<sup>2</sup>Only nMOSFETs effectively contribute to input gate leakage current. Thus, if we consider total width of only input nMOSFETs, the percentage goes down (e.g. 2.9% for  $N = 4$ ).

TABLE I  
POWER EFFICIENT HIGH  $V_t$  SWITCH

Tech. (nm)	Delay Penalty	M			
		2	4	8	16
45	3%	Header	Header	Footer	Footer
	6%	Header	Header	Footer	Footer
65	3%	Header	Header	Header	Footer
	6%	Header	Header	Footer	Footer

### C. Design of Power Optimal Current Switch

If we neglect input gate leakage currents, a header is preferred since the gate leakage current of pMOSFET is an order of magnitude smaller than that of nMOSFET [11]. However, as we discussed in the previous subsection, input gate leakage current can take up large portion of total leakage currents, and this depends on many factors: polarity (footer or header) and  $V_t$  of a current switch, delay penalty that affects the size of a current switch, the percentage of input transistors in a logic block, logic states of primary inputs when sleep, and temperature. The choice of a current switch (polarity,  $V_t$ , and size) thus lends itself to a non-obvious problem.

Specifically, in power-gated circuits with a footer, leakage current consists of subthreshold and reverse biased gate leakage current of a footer and reverse biased input gate leakage currents (for nMOSFETs whose gates are driven by primary inputs of logic 0). For power-gated circuits with a header, main leakage components are subthreshold leakage current of a header and forward biased input gate leakage currents (for nMOSFETs whose gates are driven by primary inputs of logic 1). Thus, in terms of input gate leakage current, a header is inferior to a footer since forward biased gate leakage current is larger than reverse biased one. Note that, though, this depends on input patterns, and gate leakage current of a header is negligible compared to that of a footer.

We use the same circuits in Fig. 4 to gain an understanding of the design of power optimal current switch. We change the number of gate chains, get a suitable size of a current switch depending on its polarity and delay penalty that can be tolerated, apply the randomly generated input patterns such that 1's and 0's are equally probable, and see which polarity is better for a current switch. TABLE I shows the results for 45nm and 65nm predictive technology models.

It can be seen that a header is preferred when the number of primary inputs are small. This can be understood because a footer is superior to a header in terms of input gate leakage current (reverse biased vs. forward biased), but a header is superior in terms of total leakage current of a switch itself. Thus, the benefit of a largely sized header outweighs the disadvantages of input gate leakage current. We repeat the same experiment with 65nm technology and observe the same result. We also perform the experiment with one of ISCAS benchmark circuits, called C5315, whose input transistors occupy 9.2% of total transistors. A header is recommended when a switch is

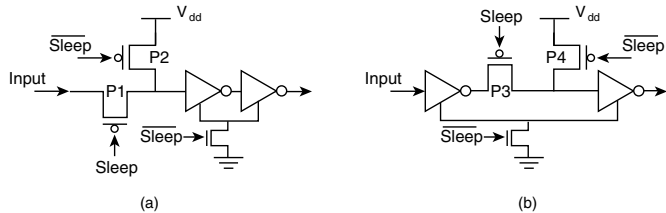


Fig. 6. Proposed circuits for input control.

sized such that 3% delay penalty can be tolerated, but a footer is superior when delay penalty exceeds 6%.

When low  $V_t$  is used for a switch, a footer is always better than a header. This is because the subthreshold leakage current of a switch now takes up large portion of total leakage currents due to its exponential dependency on the threshold voltage, and the subthreshold leakage current is smaller in a footer than in a header due to the smaller size of a footer with the same delay penalty. Thus, a footer is superior to a header in terms of its own leakage current as well as in terms of input gate leakage current.

### III. POWER OPTIMIZATION THROUGH INPUT CONTROL

Once the current switch is designed based on the method presented in the previous section, the power consumption of power gating circuits when sleep can be further reduced by controlling primary inputs. By providing logic 1 to *all* primary inputs of a power-gated circuit with a footer (similarly logic 0 in the case of a header), input gate leakage currents can be virtually eliminated.

Since the extra logic for input control can be an overhead in terms of power consumption, area, and delay, we propose two types of efficient circuits as shown in Fig. 6. In the circuit of Fig. 6(a), the input is transferred through P1 and two buffers in normal operation (i.e. when sleep=0). When sleep, the input is de-coupled to the buffers and the gate of the first buffer is driven by logic 1, which almost eliminates the gate current of the buffer. The original input transistors that are now connected to the second buffer do not induce gate currents any more, since their inputs are not directly driven by primary inputs. The main leakage component of the circuit in the sleep mode is the subthreshold leakage current of P1 when the primary input is 0, which can outweigh the advantage of input control especially when the width of P1 is large. However, this can be further reduced if high  $V_t$  is available. If we move the first buffer in front of P3 as shown in Fig. 6(b), the gate leakage current of the first buffer is now the main component of leakage current, which is in general less than the low  $V_t$  subthreshold leakage current of Fig. 6(a). The first buffer, minimum-size inverter, reduces total width of input transistors connected to primary inputs. If we replace P2 and P4 with nMOSFETs and connect their sources to ground instead of  $V_{dd}$ , we have input control circuits for a power gating circuit with a header.

We use the same circuits in Fig. 4 to see the efficiency of the

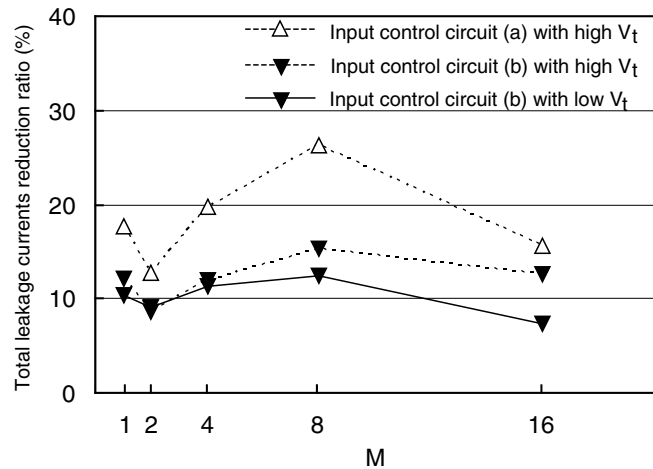


Fig. 7. Leakage current reduction with input control circuit.

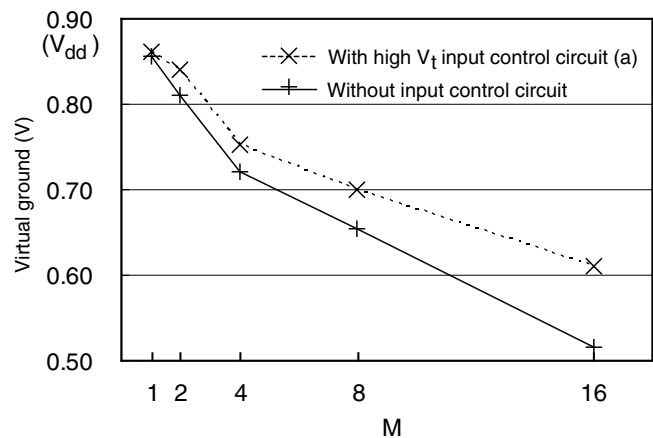


Fig. 8. Virtual ground voltage.

proposed input control circuits. We insert the input control circuit at each primary input, simulate the entire circuit (thus, the overhead of extra logic is included) to obtain the total leakage currents, and then compare them to the total leakage currents of the original circuit. Fig. 7 shows the result in the case of a footer. When high  $V_t$  is available, input control circuit in Fig. 6(a) is more efficient than that in Fig. 6(b). However, if we use only low  $V_t$ , the opposite is true.

Input gate leakage currents can be virtually eliminated by the proposed circuits. However, gate leakage current of a footer goes up due to elevated voltage of a virtual ground. This is because the extra MOSFETs in input control circuits induce current that flows through a footer in addition to the current from the logic block. Fig. 8 shows the virtual ground voltage in steady state, which clearly shows the elevated voltage with input control circuits.

We perform another experiment with a set of circuits extracted from ISCAS benchmarks and 64-b carry look-ahead adder (CLA). The current switches are sized with average cur-

TABLE II  
LEAKAGE CURRENT REDUCTION WITH INPUT CONTROL CIRCUIT

	Low $V_t$ footer	High $V_t$ footer	Low $V_t$ header	High $V_t$ header
C1908	2.0%	11.4%	-3.3%	35.3%
C2670	4.7%	22.6%	-17.1%	45.9%
C3540	7.1%	27.1%	1.1%	61.0%
C5315	8.3%	30.8%	-5.7%	52.0%
C7552	2.1%	11.9%	-8.3%	33.5%
64-b CLA	-10.2%	1.6%	-7.8%	43.7%
avg.	2.8%	19.1%	-7.4%	47.0%

rent methods [12]. For each circuit, we insert input control circuit in Fig. 6(a) when high  $V_t$  current switch is used (thus, high  $V_t$  is available), and the circuit in Fig. 6(b) otherwise. We apply randomly generated input patterns such that 1's and 0's are equally probable, and see how much leakage current can be reduced by the proposed method. TABLE II shows the result. Significant leakage reduction is observed when high  $V_t$  header or footer is used in conjunction with input control circuits in Fig. 6(a). Total leakage current increases rather than decreases in the case of low  $V_t$  header due to the overhead of input control circuits.

We measure the delay and the area of the proposed circuits. In the case of Fig. 6(a) with low  $V_t$ , the propagation delay for rising and falling inputs are 0.25ns and 0.34ns respectively. The rising and falling delays are not balanced due to the presence of pass gate (P1). The circuit of Fig. 6(b) has delays of 0.84ns and 0.65ns for rising and falling inputs respectively when all MOSFETs are in low  $V_t$ . Total width of MOSFETs in each circuit is  $1.2\mu\text{m}$ . The presence of input control circuits may or may not be an overhead. As an example, 64-b CLA in TABLE II exhibits the delay of 1.02ns and the MOSFET total width of  $654.7\mu\text{m}$ , which can be comparable to those of input control circuit. Larger circuits (e.g. C3540) may accommodate the proposed input control circuits, especially when they do not include timing critical paths inside.

#### IV. CONCLUSION

We study the influence of input gate leakage current of power gating circuits, which are widely used as a solution to suppress standby currents. It is shown that the input gate leakage current is indeed an important factor in determining the total leakage currents and varies widely depending on the polarity, threshold voltage, and size of current switch. This implies the importance of current switch design, which we also address in the paper. Finally, we propose the method of input control to reduce input gate leakage current, and propose new circuits to realize the proposed method.

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