Hardware Implementation of Super Minimum All Digital FM Demodulator

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Abstract – We propose improvement of the new architecture of digital FM demodulator. This work enhances signal quality, system clock frequency, and superior than well known PLL technique today. No more multiplier, no more ROM or table, compact size, and very fast in transient or state response. Real implementation in Altera® APEX20K200 EBC652-1X PLD gives 348 logic elements and run up to 224.42 MHz.

I. Introduction

Many efforts have been made to integrate an FM receiver on a single chip using various architectures, but the performance has been limited by analog signal processing accuracy. The main issue of integrating an FM demodulator in a chip is how to accurately discriminate a small frequency deviation of the FM signal from its center frequency. Without doubt, Phase Locked Loop (PLL) type being the most commonly use FM demodulator today. But now a new enhanced architecture which is more superior to PLL technique has been made in this work.

The new algorithm was first explained in [1] which is fall into compact size architecture, a new simple demodulation algorithm without multiplier, very fast, running without ROM or look-up table, and takes an absolute stability structure which has no feedback loop for input phase tracking.

Some improvements have been performed in this work to get better compact architecture, faster system clock, and achieve a good signal quality without FIR filter. The proposed improvement and its PLD implementation can run up to 224.42 MHz system clock using Altera® APEX20K 200EBC652-1X.

II. FM Demodulation

The new algorithm assumes that process in FM demodulation is equivalent with tracking for frequency deviation. Tracking process is performed for each period of cycle, so frequency deviation can be detected as shown in Fig.1. The gap area (D) increases along with frequency deviation magnitude. We assume that each period has 16 sampling points.

Here we try to derive this new concept with our own perception. Assume both carrier (C), and modulating signal (S_N) are harmonic signals, then

$$C(n) = A_C \cos(2\pi f_C n + \theta_C) \quad (1.1)$$

$$S_N(n) = A_S \cos(2\pi f_S n + \theta_S) \quad (1.2)$$

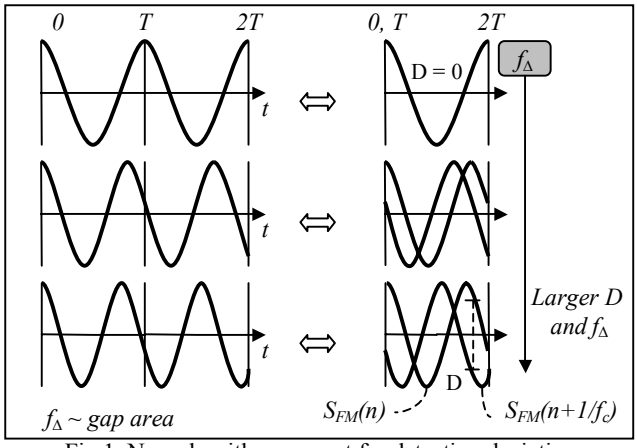

Fig.1. New algorithm concept for detecting deviation

The modulated signal (S_{FM}) will be

$$S_{FM}(n) = A_C \cos\left[(2\pi f_C + A_S \cos(2\pi f_S n + \theta_S))n + \theta_C\right] \quad (1.3)$$

From Eq.(1.3), S_N is equivalent to frequency deviation in Fig.1, thus tracking for f_Δ means demodulating S_{FM}. For tracking f_Δ, note that gap D between two signals in Fig.1 gives

$$D(n) = \left|S_{FM}(n+T) - S_{FM}(n)\right| \quad (1.4)$$

$$\Delta D(n) = D(n+T+1) - D(n) \quad (1.5)$$

$$S_N(n) = \sum_{k=-\infty}^{n} \Delta D(k) = \sum_{k=-\infty}^{n-1} \Delta D(k) + \Delta D(n) = S_N(n-1) + \Delta D(n) \quad (1.6)$$

III. Hardware Implementation

A. Improvement

The basic implementation in [1] did not take into account non linear effect of demodulation when calculating gap, D. It will exhibit high frequency components in the subtraction process in Eq.(1.4) and then accumulated in the end of demodulating process as noise that reduce demodulated signal quality. This problem actually can be solved by subjecting the output signal to low pass filter such as FIR, but it will consume large area and reduce system clock performance.

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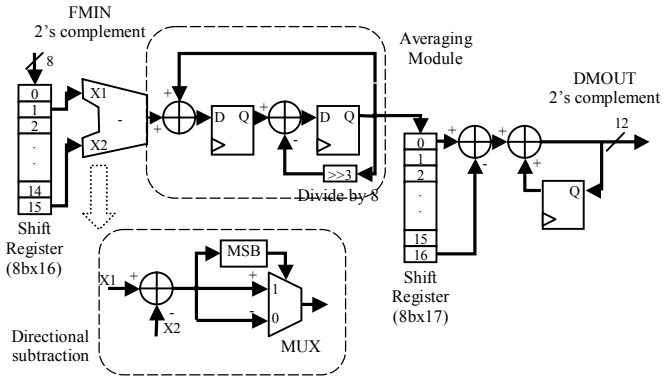


Fig.2. Improvement architecture in proposed method

The previous basic implementation in [1] used comparator to detect directional slope in computing gap *D*, and also need more adders to compensate negative value of subtraction. Our proposed method can eliminate these problems, as shown in Fig.2. Directional subtraction does not need a comparator but only need one adder. Instead of FIR filter, averaging module (loop filter) with a pole of 7/8 is added after directional subtraction to compensate non linear effect of modulation [2].

In Table.1 comparison between PLL method, basic implementation, and proposed method is given. All architectures are synthesized using Xilinx®Spartan3 3S200FT256-4 FPGA, this device is similar to device used in [1] so we can get a clear comparison. PLL has been optimized; it employs Booth's multiplier as phase detector, minimum loop filter, and optimized Numerical Controlled Oscillator (NCO) and FIR filter. Real implementation and measurement performed using Altera® APEX20K200 EBC652-1X. It gives 348 logic elements, minimum period of 4.456 ns, so it can run up to 224.42 MHz system clock frequency.

TABLE I
Synthesized result of each architecture

Architecture using Xilinx®Spartan3 3S200FT256-4	Time		Area		
	Delay (ns)	Frequency (MHz)	Slices	Slices FF	LUT
PLL (optimized)	9.725	102.828	491	548	721
Basic circuit Phase-3 [1]	6.451	155.015	184	311	48
Proposed method	4.658	214.684	195	348	61

B. Simulation and Real Waveform

Simulation in Fig.3 shows superiority of our proposed improvement method that successfully removed the ripple without loosing its quick transient and state response. In this simulation, the modulating signal is square wave with 10 KHz of frequency. We assume carrier frequency of 1 MHz with modulation index 10. System clock frequency and sampling frequency are 16 MHz.

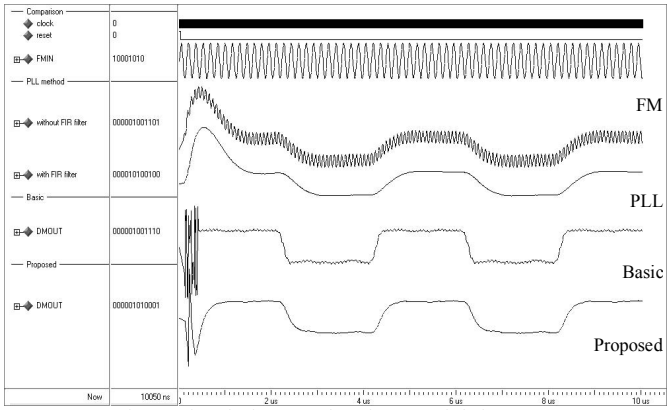
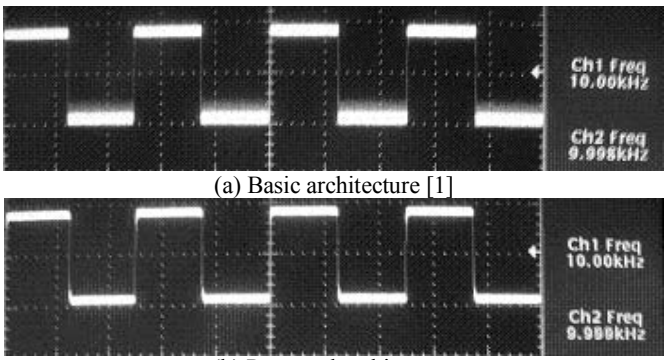


Fig.3. Simulation result using ModelSim® SE



(a) Basic architecture [1]

(b) Proposed architecture

Fig.4. Real waveform captured by oscilloscope

In Fig.4 we can see the real waveform. This waveform is taken by demodulating real FM signal generated by Leader SSG equipment signal generator.

In this real implementation, we use AD9203ARU 10-bit 40-MSPS A/D converter and THS5651AIPW 10-bit 100-MSPS D/A converter. The modulating signal is square wave signal of 10 KHz. FM signal has carrier frequency of 2.5 MHz, and system clock frequency of 40 MHz. Proposed architecture in Fig.4(b) successfully eliminates ripples shown in Fig.4(a). SNR for basic circuit is 27.8 dB while SNR for proposed method is 30.6 dB.

IV. Summary and Conclusions

This work enhanced signal quality and system clock frequency of the new architecture of all digital FM demodulator without significantly increase the area. Signal quality and high system clock frequency has become important issue of today communication systems such as software defined radio.

References

[1] Kenji Yamamoto, Masaya Yokota, "*Development of Super Minimum FM-Demodulator",* University of the Ryukyus LSI Design Contest, Okinawa, 2005.

[2] John G Proakis, Dimitris G Manolakis, "*Digital Signal Processing"*, Prentice Hall, 1996.