# A 476-gate-count Dynamic Optically Reconfigurable Gate Array VLSI chip in a standard 0.35$\mu m$ CMOS Technology

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## I. Introduction

High-speed reconfigurable processors have been developed in recent years: they are DAP/DNA chips and DRP chips [1][2]. These devices can be changed from one context to another context at every clock cycle in a few nanoseconds. However, their die size limits the number of reconfiguration contexts of currently available DAP/DNA and DRP chips to 4–16.

In contrast, optically reconfigurable gate arrays (ORGAs) [3][4] enable both fast reconfiguration and numerous reconfiguration contexts using an optical holographic memory and optical wide-band reconfiguration connections. Such devices present the possibility of large virtual gate-count VLSIs.

However, even though the virtual gate-count is extremely large, a high real gate-count is required to increase the amount of working circuits at any moment. For that reason, we previously proposed a dynamic optical reconfiguration circuit that is the smallest optical reconfiguration circuit among all ORGAs. We continue our development of high-gate-count dynamic ORGAs (DORGAs) [5].

This paper presents a new design of a fabricated 476-gate-count DORGA modified from a previously designed 68-gate-count DORGA [6] using standard 0.35 $\mu m$ three-metal CMOS process technology.

## II. Dynamic Optical Reconfiguration Circuit

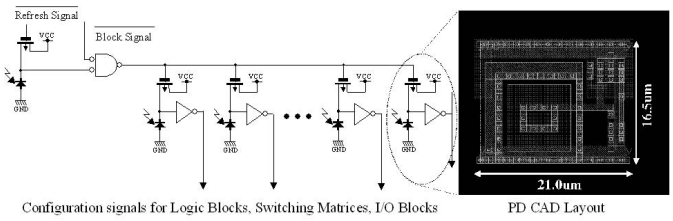


Fig. 1. Schematic diagram of an array of optical reconfiguration circuits and a CAD layout of a photodiode cell that includes a photodiode and an optical reconfiguration circuit.

A dynamic optical reconfiguration circuit that eliminates a static memory function from the VLSI part consists of only a photodiode and an inverter, as shown in Fig. 1. In that circuit, the gate array information is stored in junction capacitance of photodiodes instead of a static memory function component such as a latch, a flip-flop, or a single memory bit. Photodiodes not only detect light, but also serve as dynamic memory. The photodiode states are connected directly through inverters to the gate array component.

As a result, the dynamic optical reconfiguration circuits can be implemented in less than 10% of the area of all cell areas that comprise an optically reconfigurable logic block. The reconfiguration circuit, including the static memory function, occupied 43% of the chip area in previously proposed ORGAs [7].

TABLE I
Specification of a high-density DORGA.

| | |
|---|---|
| Technology | 0.35 $\mu m$ double-poly triple-metal CMOS process |
| Chip size | 4.9 × 4.9 [mm] |
| Supply Voltage | Core 3.3V, I/O 3.3V |
| Photodiode size | 9.1 × 8.8 [$\mu m$] |
| Distance between Photodiodes | h.=42, v.= 33 [$\mu m$] |
| Number of Photodiodes | 3,696 |
| Av. Aperture Ratio | 3.1% |
| Number of Logic Blocks | 28 |
| Number of Switching Matrices | 36 |
| Number of Wires in a Routing Channel | 8 |
| Number of I/O bits | 64 |
| Gate Count | 476 |

## III. Gate Array Design

A new 476-gate-count DORGA-VLSI chip was designed using a 0.35 $\mu m$ standard CMOS process. Table 1 shows those specifications. The respective acceptance surface sizes of the photodiode and the photodiode-cell size, including an optical reconfiguration circuit, are 8.8 $\mu m$ × 9.1 $\mu m$ and 21.0 $\mu m$ × 16.5 $\mu m$. The photodiodes were constructed between N+ diffusion and the P-substrate. The photodiode cells were arranged at 42.0 $\mu m$ horizontal intervals and at 33.0 $\mu m$ vertical intervals: 3,696 photodiodes were used. The

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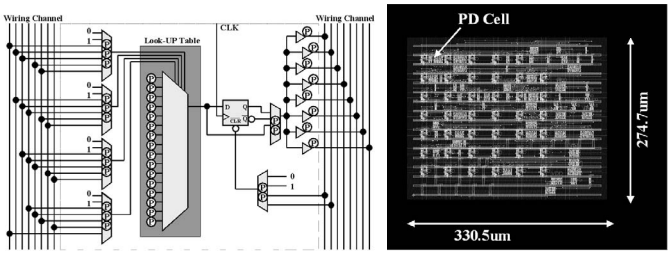


Fig. 2. Block diagram and CAD layout of an optically reconfigurable logic block (ORLB).

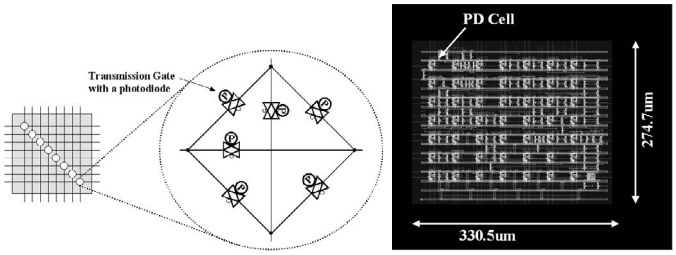


Fig. 3. Block diagram and CAD layout of an optically reconfigurable switching matrix (ORSM).

third metal layer was used for shielding transistors from light irradiation; the other two layers were used for wiring. The gate array components were designed using Design Compiler and Apollo (Synopsys Inc.), respectively, for the logic synthesis tool and the place and route tool.

Fig. 2 shows a block diagram and CAD Layout of an ORLB. The ORLB consists of a four-input look-up table (LUT), multiplexers, a D-flip flop, and tri-state buffers, along with the FPGA structure. A point of difference from FPGAs is that all states of the LUTs, multiplexers, and tri-state buffers are optically programmable through 40 photodiodes. One optical reconfiguration circuit is added to an ORLB as a block reconfiguration assignment. Therefore, 41 photodiodes were implemented in this ORLB. Wiring was executed using the first and the second metal layers while avoiding the photodiode-cell aperture area. The cell size is 330.5 $\mu m$ $\times$ 274.7 $\mu m$. Fig. 3 shows a block diagram and CAD Layout of an optically reconfigurable switching matrix (ORSM). The ORSM structure is fundamentally identical to that of units sold by Xilinx Inc., but each optical reconfiguration circuit controls a transmission gate. The cell size is 330.5 $\mu m$ $\times$ 274.7 $\mu m$.

Fig. 4 shows the CAD layout of a part of the entire gate array. The ORLBs and ORSMs are placed alternately in the horizontal direction. The ORSM cells were placed five in the horizontal direction and eight in the vertical direction. However, the corner cell was removed. The ORLB cells were placed four between ORSMs for the horizontal direction and seven in the vertical direction. In the remaining area, 16 I/O cells with 4 I/O bits were placed.

## IV. Experimental Result

The photodiode characteristics has been measured by using 633 nm He-Ne Laser. The reconfiguration period is 12 ms when each photodiode receive 505 pW laser power. In the case of reconfiguring DORGA at 100MHz, the required optical power is calculated 2.24 W since the required optical power is inverse proportion to the reconfiguration period

## V. Conclusion

This paper presented the design of the largest 476-gate count DORGA fabricated by using 0.35 $\mu m$ three-metal CMOS technology. In the case of reconfiguring DORGA at 100MHz, the required optical power was estimated 2.24 W. At that time, the reconfiguration data transfer rate of the DORGA VLSI chip reaches 369.6 Gbit/s.

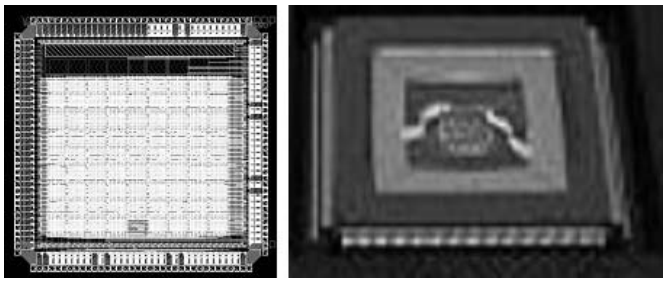

Fig. 4. The CAD layout and chip photograph.

## VI. Acknowledgments

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