Adaptively-Biased Capacitor-Less CMOS Low Dropout Regulator with Direct Current Feedback

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Abstract -- A capacitor-less low dropout regulator (LDR) with direct current feedback is proposed. A symmetrically-matched voltage mirror in sensing the load current is employed, and gives excellent line and load regulations. The dynamic biasing results in an LDR with pole-tracking that extends the bandwidth of the loop gain at high load currents. The LDR was fabricated in a 0.35μm CMOS process with an active area of 0.11mm^2, and measurement results corroborated well with both analysis and simulation.

I. Introduction

Embedding a low dropout regulator (LDR, also known as LDO) into an IC chip for on-chip power regulation can reduce the circuit board area, but bulky off-chip capacitors are usually unavoidable for adequate filtering. In addition, on-chip compensation capacitors are usually needed and this takes up valuable silicon area.

The performance of the LDR depends much on the design of the error amplifier in the voltage feedback loop. To increase the gain and bandwidth of the loop, and to eliminate the output capacitor, multi-stage amplifier with a rather sophisticated compensation scheme was proposed [1]. However, an on-chip compensation capacitor of even a few pF occupies a large silicon area, and it is better if they could further be reduced, or even eliminated. An LDR needs a large biasing current for the high-gain high-speed error amplifier for control, especially when the load current is high. It would be advantageous if the bias current of the LDR is adaptive to the load, such that at light load, the bias current is low for high efficiency, and at heavy load, the bias current is high for high speed control.

II. LDR with Direct Current Feedback

The first LDR with a dynamically biased voltage buffer was proposed in 1998 [2] but a BiCMOS process is needed and accurate current sensing was achieved due to the difference in $|V_{ds}|$ between the sensing transistor and the power transistor.

Fig. 1 shows our proposed LDR that employs an accurate current sensor using a symmetrically-matched (SM) voltage mirror [3, 4]. Two feedback loops can be identified. The scaled output voltage is compared to the reference voltage V_{ref} through an error amplifier that is simply a differential pair, and the output of which drives the pass transistor M_o to supply the load cuurent. This is the voltage feedback loop. The current feedback loop consists of the SM voltage mirror that provides a bias current I_{b2} for the error amplifier that drives M_o to complete the loop. The error amplifier is biased by M_{S5} and it sinks a current of $[2P/N]\times I_{do}$ which is the feedback current generated by the current sensor. The fed back bias current is accurately proportional to I_o, and we coined this action as direct current feedback (DCF). The drain current of the power transistor M_o bears a square relation with the gate overdrive voltage:

$$I_{do} = \tfrac{1}{2}\mu_p C_{ox} (W/L)_{M_o} (|V_{gso}| - |V_{tp}|)^2(1+|\lambda_p V_{dso}|) \qquad (1)$$

Suppose the drain current of M_o increases to $I_{do}+i_{do}$ due to an increase in load current. To accommodate this change, the gate overdrive voltage $|V_{gso}| - |V_{tp}|$ has to increase according to equation (1) to keep the output voltage constant. Now, with the ratio assignment of Fig.1, the drain current of M_{A3} increases from $(P/N)I_{do}$ to $(P/N)(I_{do}+i_{do})$, providing just the correct overdrive voltage for M_{A4} and thus, M_o. Consequently, an excellent load regulation is obtained.

For stability and bandwidth, we note that the proposed LDR has two high impedance nodes related to the feedback loops. The first one is at the output of the error amplifier V_a, and is the dominant pole $p_a = 1/(C_a R_a)$, where C_a is mainly the very large gate capacitance of M_o, and R_a is the output resistance at V_a. The second pole is at the output of the regulator V_o, with $p_o = 1/(C_o R_o) \propto I_o$, where C_o is the drain capacitance of M_o plus the parasitic capacitance of the packaging, and $R_o = r_{do}||R_L||(R_1+R_2) \propto 1/I_o$. Since the proposed LDR has no output filtering capacitor, p_o is much larger than p_a. Now, the criteria of design is to make sure that p_o is higher than the unity gain frequency ω_t due to the single pole roll-off of p_a, and $\omega_t = bg_{mA1}g_{mo}R_o/C_a$. M_{A1} and M_{A2} are designed to work in weak inversion region at light to medium load such that $g_{mA1} \propto I_o$ [5]. At light load, M_o works in weak inversion region also and $g_{mo} \propto I_o$, giving $\omega_t \propto I_o$. The unity gain bandwidth tracks with p_o. At medium load, M_o works in strong inversion region such that $g_{mo} \propto \sqrt{I_o}$, while M_{A1} and M_{A2} are designed to stay in weak inversion region, thus $\omega_t \propto \sqrt{I_o}$. The bandwidth ω_t is still extending with the load current but at a slower rate. At heavy load, M_{A1}, M_{A2} and M_o work in strong inversion region, and g_{mA1}, $g_{mo} \propto \sqrt{I_o}$, giving ω_t independent of I_o. Separation between ω_t and p_o becomes larger as I_o increases. As a result, if the LDR is stable at a light load current, it is guaranteed to be stable at a higher load current.

III. Simulation and Measurement Results

The direct current feedback low dropout regulator was fabricated in a 0.35μm CMOS process. Fig.2 shows the simulated loop gain response. Pole tracking is evident as both p_a and p_o move to higher frequencies at a high load current, with p_o moves faster than p_a, and the unity gain bandwidth is extended. Fig.3(a) shows the measured load transient response of the DCF LDR with a current step of 1mA to 150mA. For a load change from high to low, the initial large bias current gives a fast response and the ripple is small, only 4mV, and is even smaller than 0.5% of the output voltage. For a load change from low to high, the initial bias current of the error amplifier is small and the response is slow and leads to a larger glitch of 50mV at the output. As the bias current increases with the load current, the bandwidth increases and the output voltage is stabilized very quickly. The 1% settling time (18mV of 1.8V) is less than 200ns. Fig.3(b) shows the rejection of switching noise. In this measurement, the LDR is cascaded to a switching converter. Low frequency ripples are filtered out effectively and high frequency glitches are attenuated by approximately 14dB. Fig.4 shows the measured output voltage vs the load current and the supply voltage. For a load current that changes from 0 to 240mA at V_{dd} = 2.2V, the load regulation is only

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2.77μV/mA (664μV in total). Note that for a conventional LDR, the output voltage decreases monotonically as the load current increases, but for the proposed DCF LDR, the output voltage increases initially at light load current, which is due to the current feedback mechanism using the symmetrically-matched voltage mirror, and the load regulation is not solely controlled by the gain of the error amplifier. Fig.5 shows the measured quiescent current I_q vs the load current I_o. The quiescent current includes the currents consumed by the error amplifier, the voltage mirror and the feedback resistors. At light loads, I_q is closed to I_{b1} (a very small bias current in case the load current goes to zero) plus the current of the potential divider, but as I_o is larger than 1mA, I_q increases linearly, which implies that the current sensor works properly. Table 1 summarizes the specifications of the proposed DCF LDR. Fig.6 shows the chip micrograph.

IV. Conclusions

We demonstrated a working low dropout regulator that employed adaptive biasing and symmetrical matching techniques. Remarkable performance in both load transient response and load regulation are shown in the measurement results. The resultant LDR needs no filtering and compensation capacitors, and fabrication cost could be much reduced. Therefore, it is suitable for system-on-chip (SOC) applications and as an on-chip power regulator.

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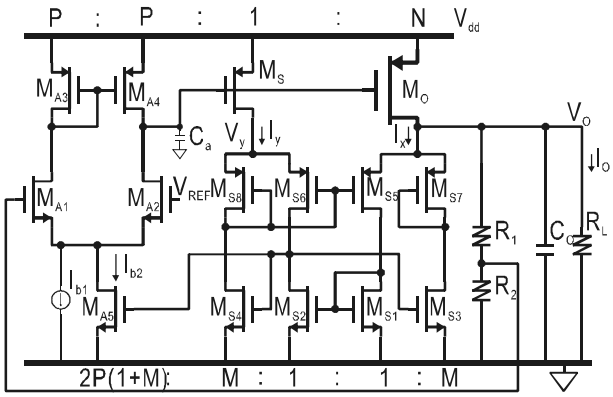

Fig. 1 Schematic of DCF LDR

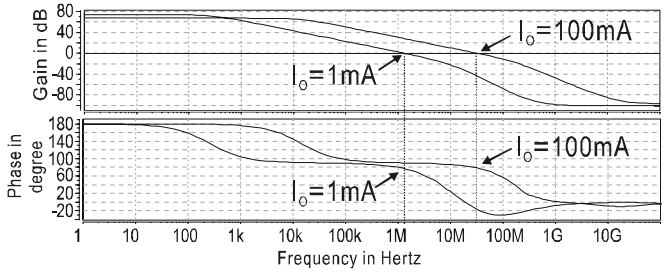

Fig. 2 Loop gain simulation of DCF LDR

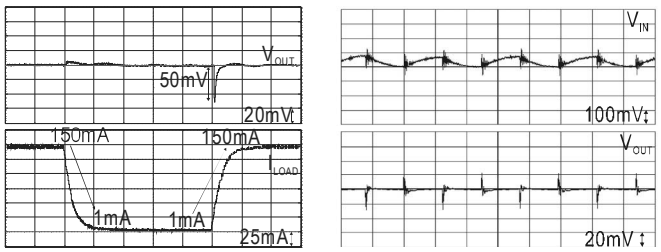

Fig. 3 (a) Load transient response in load change between 1mA and 150mA (2μs/div) and (b) Line ripple rejection with high frequency switching noise

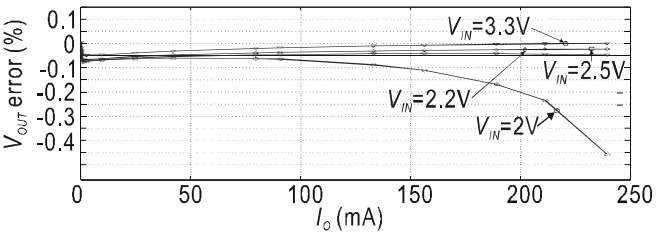

Fig. 4 Load regulation of the DCF LDR

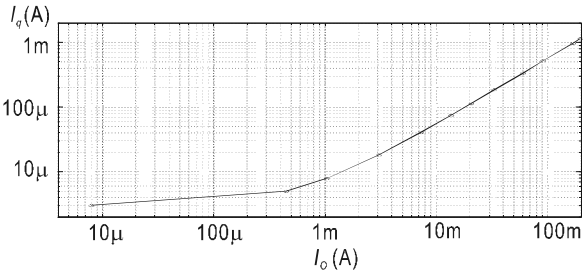

Fig. 5 Quiescent current versus load current

TABLE 1
SPECIFICATIONS OF THE DCF LDO REGULATOR

Technology	0.35μm CMOS process
Chip area (including pads)	0.32 mm²
Chip area (active circuit area)	0.11mm²
V_{dd}	2-3.6V
V_O	1.8V
Maximum I_O	240 mA
Quiescent Current @ I_O=0mA	3 μA
Quiescent Current @ I_O=200mA	1.03 mA
Load regulation @ V_{dd}=2.2V, I_O=0mA to 240mA	2.77μV/mA (664μV total)
Line regulation @ V_{dd}=2V to 3.6V, I_O=100mA	<0.8mV/V (1.28mV total)
Line ripple rejection @ 10kHz	>40 dB
Output impedance @ 1MHz (I_o=100mA)	200mΩ

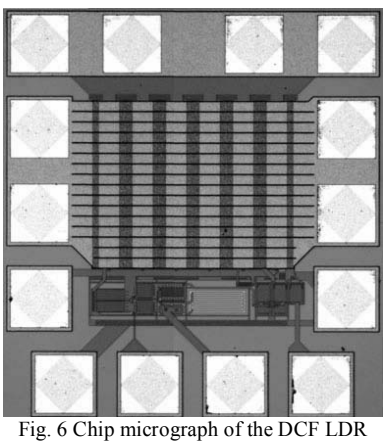

Fig. 6 Chip micrograph of the DCF LDR