An Implementation of a CMOS Down-Conversion Mixer for GSM1900 Receiver

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***Abstract*—A 1.9-GHz down-conversion CMOS mixer, intended for the GSM1900 (PCS1900) Low-IF receivers is present with the utilization of novel folded Gilbert Cell fabricated in a RF 0.18-µm CMOS process. The prototype demonstrates a good performance. It achieves a conversion gain of 6dB, SSB Noise Figure of 18.5dB and IIP3 11.5dBm while consuming 7mA current from 3.3V power supply.**

I. INTRODUCTION

This paper presents the design and the implementation of a high CMOS frequency down-conversion mixer suitable for a single-chip receiver as shown in Fig. 1. The receiver topology proposed here is designed for the Personal Communications Standard (PCS1900) that operates at central frequency of 1.9GHz designating the receiver band from 1930MHz to 1990MHz.

The proposed mixer here is based on a novel folded Gilbert cell topology shown in Fig.3. This mixer topology is similar to the classical Gilbert cell based mixer (Fig.2). Virtually one of the main advantages of the proposed topology is to use tank circuits to fold the RF signal to the switching pairs, thus retains the same advantages as the Gilbert cell based mixer. Meanwhile with this folded topology we can set the bias current of the trans-conductance stage and the commutate stage independently, thus the noise and linearity performances can be optimized independently, also the P-MOSFET commutate stage suffers less 1/f noise which sometimes dominates the noise performance of the mixer in the Low-IF systems [2] [3] [4]. Section 2 will describe the design of this down-conversion

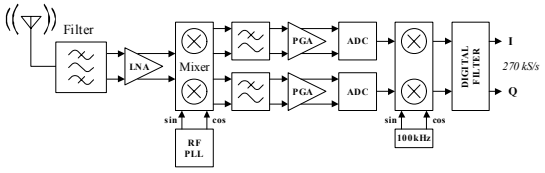

Fig.1 GSM1900 Low-IF Receiver architecture

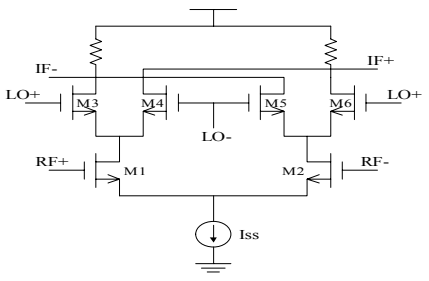

Fig.2 Topology of the traditional Gilbert cell of a mixer

mixer in more details. It is followed by Conclusions in Section 4.

II. DESIGN OF THE MIXER

2.1 Principles and Design considerations

The schematic of the proposed mixer is shown in Fig. 3 and Fig. 4 respectively, including a mixer core, a LO buffer and the bias circuits. In the mixer core design, M3-M6 PMOS cross-coupling cells are designed as mixer current commutation stage and M1, M2 NMOS pairs as trans-conductance stage. Two inductors Ld1, Ld2 co-operate with C1, C2 (including the parasitic capacitances) of point X and Y, which ensure to resonate at the central frequency of the input signal. Two off-chip resistors are employed as output IF loads to facilitate the testing. Ls1 and Ls2 are two inductors used as inductively degenerates that are similarly used in the LNA input stage. These inductors are both good for the conjugate matching of mixer input and the linearity performance [1].

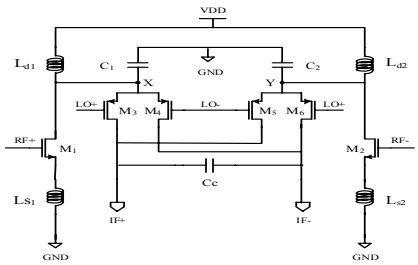

Fig.3. The proposed mixer core circuit with folded topology

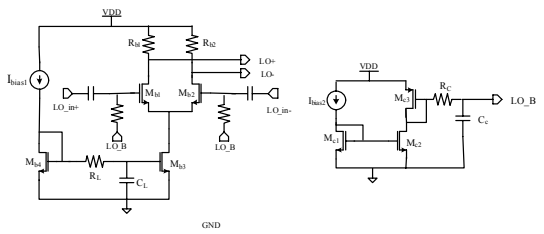

Fig.4 The LO buffer and the bias circuits

III. IMPLEMENTATION AND MEASUREMENTS

The GSM1900 Receiver was fabricated in SMIC 0.18-µm CMOS RF technology. The die micrograph of mixer is shown in Fig 5. The active area of the mixer with LO Buffer is 0.8mm×0.7mm. The testing instruments include Spectrum Analyzer E4440A, Vector Network Analyzer E5071B, RF signal generator E4438C and Noise Source E346C from Agilent Technologies™. The measured performance of the mixer is summarized in Table 1. Fig 6 shows the measured

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output spectrum of the mixer. Considering the losses of the microwave connector and the single to differential Balun, the conversion gain of the mixer at 100kHz IF is around 6dB. In order to evaluate the linearity of the mixer, two-tone inter-modulation measurement was carried out with tone frequencies at 1900MHz and 1900.2 MHz respectively. Fig.7 and Fig.8 show the 1-dB compression point and IIP3 results respectively. Due to the equipment limitation, the SSB noise figure of the mixer can only be measured at 1MHz(instead of 100kHz) IF output and shows 18.5dB(include the noise effects of an off-chip output buffer and the LO buffer).

TABLE I. SUMMARY OF MIXER MEASUREMENTS

Mixer	Measured Parameters
Supply voltage	3.3V
Current dissipation	7mA
RF frequency	1900MHz
LO frequency(4dBm)	1900.1MHz
SSB(Noise Figure)	18.5dB
Power Conversion Gain	6dB
Input IP3	11.5dBm
Input P- 1dB	1.5dBm
LO-RF feed-through	-53dB
LO-IF feed-through	-48dB

IV. CONCLUSIONS

A 1.9-GHz down-conversion CMOS Mixer with the utilization of novel folded Gilbert Cell fabricated in a RF 0.18-μm CMOS process has been described. With this folded mixer, the bias current of the trans-conductance stage and the switching stage can be set independently to get an optimization of both linearity and noise performances. The mixer modular, includes a mixer core and a LO buffer, achieves a conversion gain of 6dB, Noise Figure of 18.5dB and IIP3 of 11.5dBm while consuming only 7mA current from 3.3V power supply. The measurement results show that the performance of this mixer has met the requirements of the low-IF GSM1900 receiver system.

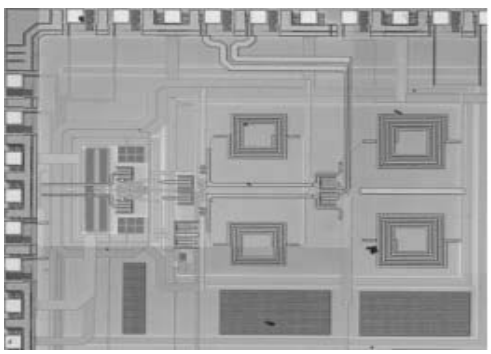

Fig.5 Micrograph of the mixer die

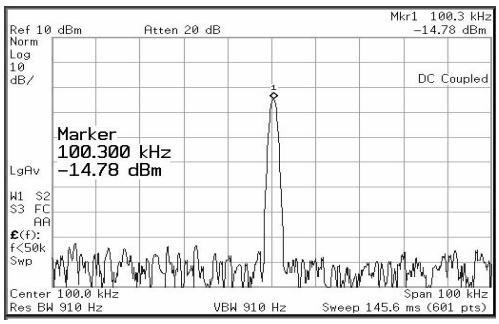

Fig.6 Measured mixer output spectrum: RF input power -20dBm/1900MHz and LO power 4dBm/1900.1MHz

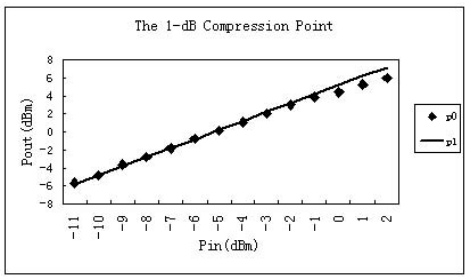

Fig.7 Measured P1-dB Compression Point of the mixer

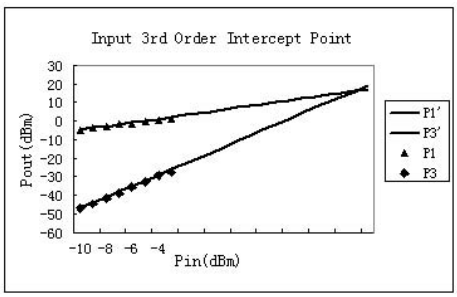

Fig.8 Extrapolation of the mixer IP3

ACKNOWLEDGMENT

The major works were finished at Fudan-Sicomm Union-Laboratory. The authors thank Shanghai Sicomm RF Technology, Inc. for the support on system specification, circuit design, the devices modeling and circuit testing. Besides, the authors thank the team members Junbiao Ding, Fang Yang , Zhisheng Li and Jiasheng Hu for the cooperation.

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