ENTITY And2 IS
PORT (a: IN std_logic;
b: IN std_logic;
F: OUT std_logic);
END And2;

ARCHITECTURE And2_beh OF And2 IS
BEGIN
PROCESS(a,b)
BEGIN
F <= a AND b AFTER 2.4 NS;
END PROCESS;
END And2_beh;

ENTITY Or2 IS
PORT (a: IN std_logic;
b: IN std_logic;
F: OUT std_logic);
END Or2;

ARCHITECTURE Or2_beh OF Or2 IS
BEGIN
PROCESS(a,b)
BEGIN
F <= a OR b AFTER 2.4 NS;
END PROCESS;
END Or2_beh;

ENTITY Inv IS
PORT (a: IN std_logic;
F: OUT std_logic);
END Inv;

ARCHITECTURE Inv_beh OF Inv IS
BEGIN
PROCESS(a)
BEGIN
F <= NOT a AFTER 1 NS;
END PROCESS;
END Inv_beh;
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Testbench IS
END Testbench;

ARCHITECTURE TBarCh OF Testbench IS
  COMPONENT And2 IS
    PORT (a: IN std_logic;
          b: IN std_logic;
          F: OUT std_logic);
  END COMPONENT;

  SIGNAL a_s, b_s, F_s: std_logic;

  BEGIN
    CompToTest: And2 PORT MAP (a_s, b_s, F_s);

    PROCESS
    BEGIN
      -- Test all possible input combinations
      b_s <= '0'; a_s <= '0';
      WAIT FOR 10 ns;
      b_s <= '0'; a_s <= '1';
      WAIT FOR 10 ns;
      b_s <= '1'; a_s <= '0';
      WAIT FOR 10 ns;
      b_s <= '1'; a_s <= '1';
      WAIT;
    END PROCESS;
  END TBarCh;