LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Sel2 IS
  PORT (d0, d1: IN std_logic;
        s: IN std_logic;
        Y: OUT std_logic);
END Sel2;

ARCHITECTURE Sel2_beh OF Sel2 IS
BEGIN
  PROCESS(d1, d0, s)
  BEGIN
    IF (s='0') THEN
      Y <= d0;
    ELSE
      Y <= d1;
    END IF;
  END PROCESS;
END Sel2_beh;
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Sel2 IS
    PORT (d1, d0: IN std_logic;
        s: IN std_logic;
        Y: OUT std_logic);
END Sel2;

ARCHITECTURE Sel2_str OF Sel2 IS
    COMPONENT And2 IS
        PORT (a, b: IN std_logic;
            F: OUT std_logic);
    END COMPONENT;

    COMPONENT Or2 IS
        PORT (a, b: IN std_logic;
            F: OUT std_logic);
    END COMPONENT;

    COMPONENT Inv IS
        PORT (a: IN std_logic;
            F: OUT std_logic);
    END COMPONENT;

    BEGIN
        Inv_1: Inv PORT MAP (s, w1);
        And2_1: And2 PORT MAP (d0, w1, w2);
        And2_2: And2 PORT MAP (d1, s, w3);
        Or2_1: Or2 PORT MAP (w2, w3, Y);
    END Sel2_str;
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Testbench IS
END Testbench;

ARCHITECTURE TBarch OF Testbench IS
  COMPONENT Sel2 IS
    PORT (d1, d0, s: IN std_logic;
          Y: OUT std_logic);
  END COMPONENT;

  SIGNAL d1_s, d0_s, s_s, Y_s: std_logic;

  BEGIN
    CompToTest: Sel2
      PORT MAP (d1_s, d0_s, s_s, Y_s);

    PROCESS
      BEGIN
        d1_s <= '0'; d0_s <= '0'; s_s <= '0';
        WAIT FOR 10 ns;
        d1_s <= '0'; d0_s <= '1'; s_s <= '0';
        WAIT FOR 10 ns;
        d1_s <= '0'; d0_s <= '1'; s_s <= '1';
        WAIT FOR 10 ns;
        d1_s <= '1'; d0_s <= '1'; s_s <= '1';
        WAIT;
      END PROCESS;
  END TBarch;