Principles Of Digital Design

Discussion: Flip-Flops

D-Latch Design Latch vs. Flip-Flop Timing

D-latch Design

 Design a gated D-latch using NAND gates and inverters. Draw the schematic and create a truth table for it. An implementation of simple gates is provided for reference.



Latch and Flip-Flop Comparison

- Compare the behavior of D latch and D flip-flop devices by completing the timing diagram in the figure below. Assume each device initially stores a 0.
 - Latches are level-sensitive since they respond to input changes during clock width. (e.g. when clock is 1)
 - Flip-Flops respond to input changes only during the change in clock signal, (e.g. at rising edge of clock signal)



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