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Source Re-coding to Create Parallel and Flexible MPSoC Models for Embedded System Design and Exploration

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To overcome the complexity in Multi-Processor System-on-Chip (MPSoC) design, researchers have developed sophisticated methodologies and design flows that significantly reduce the development time through automation. Given a suitable input SoC model, ESL tools today are effective in generating efficient implementations. While much work has focused on synthesis and exploration tools, little has been done to support the designer in writing and rewriting SoC models. In fact, our studies on industrial size examples have shown that about 90% of the system design time is spent on coding and re-coding of SLDL models, even in the presence of algorithms given in the form of C code. Since the quality of the design model has tremendous impact on the cost and quality of the resulting system implementation, creating and optimizing the model is a critical task toward successful SoC design.

Re-using readily available C algorithms can speed-up the SoC design process. However, readily available reference C codes are not conducive for system synthesis as they lack the necessary characteristics such as parallelism, structural hierarchy, analyzability and synthesizability. The reference C codes lack proper isolation of computation and communication, lack parallelism, contain intractable pointers and unanalyzable control structures, which render today's ESL tools ineffective. Reusing these C sources for creating SoC models require significant non-trivial re-coding, which could result in sub-optimal models if not done correctly. The lack of sufficient automation help to create these models requires that designer manually implement this re-coding, which is tremendously time-consuming and error prone.

This dissertation focuses on this automation-gap, which is widely prevalent across many system-level design flows today. To overcome this automation gap, we present our novel "Recoding" approach, which efficiently combines the automation with the designer's application-specific knowledge. In this approach the overall task of creating the SoC model from C reference code is achieved through iterative application of recoding transformations. In this thesis we present several source-level code transformations to create a suitable SoC model. Our code transformations address aspects such as separating computation and communication, code parallelization, code partitioning and code restructuring. An interactive source re-coder integrates these static analysis and code transformation tools into an editor, to assist the designer in tedious modeling and optimization tasks. This refactoring approach to create efficient SoC models allows the designer to use her/his limited modeling time efficiently, and makes the whole approach feasible on real-life source codes. This automation not only helps the designer in creating models faster, but also enables the designers to quickly realize different models and compare the trade-offs and benefits of each type of model. By having control over the type and scope of the transformation, designer can use these generic transformations to create models acceptable to the design flow and most suitable for the underlying platform.