

INDUSTRIAL SPEAKER SERIES

Center for Embedded Computer Systems

Presents

Programming FPGA in C using ROCCC

Jason Villarreal, Adrian Park, Roby Atadero
Jacquard Computing Inc.
Riverside, CA

Walid Najjar
University of California, Riverside
Riverside, CA

Abstract

ROCCC (Riverside Optimizing Compiler for Configurable Computing) is a C to VHDL compilation framework specifically focused on FPGA-based code acceleration. Its focus is on compile time transformations and optimizations aimed at generating an efficient circuit from a loop nest. Its objectives are to maximize parallelism within the constraints of the target device, optimize clock cycle time by efficient pipelining and minimize the area utilized. Furthermore, ROCCC relies on extensive and unique loop analysis techniques to increase the reuse of data fetched from off-chip memory. ROCCC 2.0 is a free and open source tool that supports a modular bottom-up approach to the programming of FPGA accelerators, supporting code reuse at multiple levels while maintaining full compatibility with C. It has been ported to several platforms including Xilinx development boards and the Convey Computers HC-1.

About the company:

Jacquard Computing provides technical service in the development of novel accelerated applications and porting of ROCCC 2.0 to FPGA platforms. ROCCC 2.0's free and powerful tool set is the tool to use for C to VHDL solutions.

The team at JCI has more than 15 years combined experience in compilation of high level languages to FPGA-based hardware accelerators. Their goal is to provide the tools and services needed for their customers to fully take advantage of the untapped parallel nature of reprogrammable hardware.

Thursday, October 6, 2010

Calit2 3009

Tutorial begins at 10:00am; Refreshments at 9:30am

CECS Host: Fadi Kurdahi

For more information contact: Melanie Kilian at (949) 824-9127

UNIVERSITY OF CALIFORNIA, IRVINE