

INDUSTRIAL SPEAKER SERIES

Center for Embedded Computer Systems

Presents

STP Engine, a C-based Programmable HW Core featuring Massively Parallel and Reconfigurable PE Array: Its Architecture, Tool, and Real System Usecases

Dr. Masato Motomura
System IP Core Research Laboratories, NEC Corporation
Tokyo, Japan

Abstract

Stream Transpose (STP) Engine is a programmable HW core to accelerate stream processing in modern system LSIs. It is composed of an array of numerous numbers of processing and memory elements as well as an intelligent data streaming HW mechanism. Key differentiation from other may-core type parallel architectures lies in its programming model: i.e., a design tool based on high-level HW synthesis technology compiles a C source code into a set of pseudo HW configurations which are spatially and temporally mapped onto the array. The STP engine is productized in 90nm-generation system LSIs, and is targeted for wider-range use in forthcoming generations beyond 40nm.

Biography

Dr. Motomura received EE doctoral degree from Kyoto University in 1996. He has been engaged in research of various LSI architectures, such as functional memories, parappel processors, and reconfigurable arrays in NEC research laboratories since 1987. From 2002 to 2009, he led technology and business development of STP Engine in NEC Electronics. He was also the winner of 1992 IEEE JSSC Best Paper Award. LSI

Monday, December 14, 2009

Donald Bren Hall 3011

Talk begins at 2:30pm; Refreshments at 1:30pm

CECS Host: Nikil Dutt

For more information contact: Melanie Kilian at (949) 824-9127

UNIVERSITY OF CALIFORNIA, IRVINE