

# INDUSTRIAL SPEAKER SERIES

## Center for Embedded Computer Systems

*Presents*

### **Challenges in compiling for modern architectures**

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In the last two decades the computer architecture performance was relying on frequency. However, as the frequency race seems to reach its physical limitations, the real challenge is how to keep on improving the performance in respect to the "Moore's Law". New architectural ideas are introduced, such as the use of multi-threading, multi cores architectures including homogeneous and heterogeneous ones (like the Cell processor).

What does this mean for their usability? How this influence the software development cycle? What kind of challenges they impose on compilers? In the talk I will address these issues and discuss some new research directions.

*Bilha Mendelson is a manager of the Code Optimization Technology department in the IBM Haifa Research Lab, Israel. Since joining IBM in 1990, she has been developing optimizations for DSP compiler and for the AS/400 optimizing translator. She received a B.Sc. and an M.Sc. in Computer Science from the Technion, Israel Institute of Technology, and a Ph.D. in Computer Engineering from the University of Massachusetts at Amherst. She also received an MBA from the Haifa University in Israel. She holds several patents primarily in the area of code optimization. Her areas of interest include code optimization algorithms, compiler technology, computer architecture, and performance improvement issues.*

### **How many cores is too many cores?**

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The computer industry has been able to keep an exponential improvement in performance for the last few decades. This unbelievable phenomenon is known as "Moore's law". As the computer architecture industry start reaching the "power wall", two new trends are developed; the first trend calls to trade single thread performance with multithreaded performance and so to increase the overall performance of a processor by accommodate it with large number of small cores. The second trend calls to increase both the single thread performance and the multithreaded performance and so to divide the "transistor budget" of the processor between relatively small number of "large cores".

In this talk I will present the root cause of the "power wall", I will extend the discussion on each of the new trends in computer architectures described above and provide an analysis of what is needed for each of them to succeed. I will conclude the talk with a discussion on few open research topics which I believe are important for the computer architecture industry.

*Avi Mendelson is a principal engineer in Intel's Mobile Platform Group in Haifa, Israel, and adjunct professor in the CS and EE departments, Technion – Israel Institute of Technology. He received his B.Sc. and M.Sc degrees from the Technion, Israel Institute of Technology and his PhD from the University of Massachusetts at Amherst. Avi has been with Intel for 7 years. He started as senior researcher in Intel Labs, later he moved to the Microprocessor group where he served as the CMP architect of Intel Core Duo. Avi's work and research interests are in computer architecture, low power design, parallel systems, OS related issues and virtualization.*

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