

Date: August 24, 2004

To: William H. Parker
Vice Chancellor for Research
Dean of Graduate Studies

From: Daniel D. Gajski
Henry Samueli "Turing" Endowed Chair
Director, Center for Embedded Computer Systems

Subject: CECS 2003-2004 Annual Report

The Center for Embedded Computer Center {CECS} ended the 2004 fiscal year with many significant accomplishments and a strong and innovative research program. CECS is internationally recognized as an outstanding research center in embedded systems.

The core and domain research programs were conducted by 22 UCI faculty members and 50 graduate students. Dr. Mutsuhiro Arinobu, Vice President, Toshiba Corporation, Tokyo, Japan became a member of the CECS Research Advisory Board. Today, we have three distinguished industrial executives serving on the CECS Research Advisory Board. We treasure and value the research advice and guidance from this distinguished group of industrial executives. We also sponsored 4 CECS Distinguished Lectures which brought outstanding professors to our center to interact with our graduate students. We also hosted 17 research visitors from foreign industry and universities who conducted embedded systems research for varying time periods.

As recognition of our research capabilities, we were successful in capturing \$4,466,136 in contracts and grants, and \$1,074,305 in research donations for a total of \$5,540,441. The funding highlight of the fiscal year was the awarding of a \$3,300,000 to Professor Daniel D. Gajski to develop a space electronics design methodology. This level of research funding and support signifies the importance of and the recognition achieved by our core and domain research programs.

Four issues of CECS eNEWS were published this calendar year which pictorially highlighted the research accomplishments of our faculty members, graduate students, and visitors. We also held the Southern California Embedded Systems Symposium (SCESS) which showcased our leading-edge research to the Orange County technical community. The SCESS Keynote Address was delivered by F. Matthew Rhodes, President, Conexant Systems, Inc. to 120 attendees.

Thirty five CECS Technical reports were published and posted on the CECS web site covering a variety of research topics. Our web site, www.cecs.uci.edu, was maintained in a timely manner and the site navigation was dramatically improved. Our home page was completely redesigned with rotating pictorial presentations depicting CECS events.

Our core and domain research programs were extremely successful in fiscal year 2003/2004. We are striving to build on these research accomplishments in 2005 hoping to have significant societal impact through innovative research and technology transfer.

FACULTY MEMBERS

Nader Bagherzadeh - Electrical Engineering and Computer Science, UC Irvine
Lubomir Bic - Information & Computer Science, UC Irvine
Pai H. Chou - Electrical Engineering and Computer Science, UC Irvine
Nikil D. Dutt - Information & Computer Science, UC Irvine
Daniel D. Gajski - Information & Computer Science, UC Irvine
Jean-Luc Gaudiot - Electrical Engineering and Computer Science, UC Irvine
Tony Givargis - Information & Computer Science, UC Irvine
Rajesh K. Gupta - Computer Science & Engineering, UC San Diego
Raymond Klefstad - Electrical Engineering and Computer Science, UC Irvine
Fadi Kurdahi - Electrical Engineering and Computer Science, UC Irvine
Kwei-jay Lin - Electrical Engineering and Computer Science, UC Irvine
J. Michael McCarthy - Mechanical Engineering, UC Irvine
Alex Nicolau - Information & Computer Science, UC Irvine
Alex Orailoglu - Computer Science & Engineering, UC San Diego
Tatsuya Suda - Information & Computer Science, UC Irvine
Bruce J. Tromberg - Beckman Laser Institute, UC Irvine
Frank Vahid - Computer Science & Engineering, UC Riverside
Alexander Veidenbaum - Information & Computer Science, UC Irvine

NEW FACULTY MEMBERS (FY 2003/04)

Rainer Doemer – Electrical Engineering and Computer Science, UC Irvine
Ian Harris - Information & Computer Science, UC Irvine
Payam Heydari - Electrical Engineering and Computer Science, UC Irvine
Isaac Scherson - Information & Computer Science, UC Irvine

RESEARCH ADVISORY BOARD MEMBERS

Dr. Gilbert F. Amelio - Senior Partner, Sienna Ventures, Sausalito, California
Dr. Mutsuhiro Arinobu – Vice President, Toshiba, Tokyo, Japan
Dr. Jai H. Hakhu – Vice President, Intel, Santa Clara, California

ADMINISTRATION and RESEARCHER

Daniel D. Gajski - Director
Robert Larsen - Associate Director
Juancho Banaag - Assistant Director
Quent Cassen - Research Relations
Christina Dinh - Financial Analyst
Quoc-Viet Dang - Programmer Analyst/Web Developer
Maral Melkichian - Student Assistant
Lukai Cai - Project Scientist
Andreas Gerstlauer - Project Scientist

ADMINISTRATION and RESEARCH (continue)

Sumit Gupta -Project Scientist
 Prahbat Mishra - Project Scientist
 Junyu Peng - Project Scientist
 Dongwan Shin - Project Scientist

VISITORS

Yohei Akita - Hitachi Limited, Tokyo, Japan
 Juan Luis Aragon - University of Murcia, Murcia, Spain
 Kiyong Choi - Seoul National University, Seoul, South Korea
 Akira Fukuda - Kyushu University, Fukuoka, Japan
 Tak-Don Han - (EECS visitor – Kane Kim)
 Takaaki Imai - Renasas Technology Corporation, Tokyo, Japan
 Su-Chong Joo - (EECS Visitor – Kane Kim)
 Han-Gyoo Kim - Hong-IK University, Seoul, South Korea (EECS visitor of Kane Kim)
 Sunghyun Lee - (Dutt ICS visitor)
 Hyunok Oh - Seoul National University, Seoul, South Korea
 Chun-Myoung Park - Chungju National University, Chungju, South Korea
 Wolfgang Rosenstiel - University of Tuebingen, Tuebingen, Germany
 Marc Sabate' - University Polytechnic of Catalunya, Spain
 Wonyong Sung - Seoul National University, Seoul, South Korea
 Oriol Ventura - University Polytechnic of Catalunya, Spain
 Hiroyuki Yagi - Sony Corporation, Tokyo, Japan
 Whanki Yong - Handong Global University, Gyoung-buk, South Korea

GRADUATE STUDENTS

Samar Abdi	Ravindra Jejurikar
Yuvraj Agarwal	Arun Kejariwal
Carmen Badea	Jihye Kim
Sudarshan Banerjee	Sung Jun Kim
Nikhil Bansal	Kyoungwoo Lee
Partha Biswas	Li Lihua
Srinivas Bongoni	Rafael Lopez
Marcio de Oliveira Buss	Atri Mandal
Pramod Chandraiah	Mahesh Mandipaka
Han-su Cho	Chhawchhari Manjari
Siddharth Choudhuri	Ravindran Mohavelu
Radu Cornea	Pinikai Mukherjee
Paolo D'Alberto	Andre Nacul
Ambarish De	Dan Nicolascu
Mohammaed Ghodrat	Sudeep Pasricha
Arijit Gosh	Mukesh Rajan
Ashok Halambi	Kiran Ramineni
Ilya Issenin	Mohammad Reshadi

GRADUATE STUDENTS (continue)

Amir Safarian
Nick Savoii
Eun Kyong Seo
Srikanth Srinivasan
Aviral Shrivastava
Weiyu Tang
Bo Tian
Jelena Trajkovic

Anshuman Tripathi
Shireesh Verma
Ahmad Yazdi
Haobo Yu
Ying Zhang
Shuqing Zhao

STUDENT INTERNS

Issenin Ilya – IMEC
Rafael Lopez – AGEF
Manev Luthra – ATHEROS
Sudeep Pasricha - Connexant, Newport Beach, California
Aviral Shrivastava – Intel Corporation,

GRADUATED STUDENTS

Lukai Cai, Ph.D.
Andreas Gerstlauer, Ph.D.
Sumit Gupta, Ph.D.
Manev Luthra, MS
Prabat Mishra, Ph.D.
Junyu Peng, Ph.D.
Dongwan Shin, Ph.D.

PROPOSAL SUBMITTED

Eleven proposals submitted to various Federal, Private and Industrial agencies amounting to \$5,597,744.

SPACE ALLOCATIONS

CECS has space allocation in Information and Computer Science and Engineering Research Facility Building (IERF). It provides office and lab space for 5 faculty members, 52 students, 7 administrative staff, 6 project researcher and 17 visitors (during FY2003/04).

AWARDED CONTRACTS AND GRANTS

Semiconductor Research Corporation	\$209,793
UC Micro State (2001)	1,177
UC Micro Intel (2001)	48,805
UC Micro State (2002)	15,615
UC Micro Intel (2002)	50,834
UC Micro State (2003)	34,500
UC Micro Intel (2003)	40,000
UC Micro State (2003)	11,458
UC Micro Conexant (2003)	30,000
UCLA/Semiconductor Research Corporation	60,000
National Science Foundation/NSG	255,752
National Science Foundation/INRIA, France	36,166
National Science Foundation	94,275
National Science Foundation/DA	25,380
Toshiba, Japan	38,275
InterDesign Technologies, Japan	3,410,325
Hitachi, Ltd., Japan	83,904
STARC, Japan	19,877
Sub Total	\$4,466,136

RESEARCH DONATIONS

Motorola, Incorporated	825,834
Semiconductor Research Corporation	8,686
SpecC Technology Open Consortium, Japan	19,388
InterDesign Technology, Incorporated, Japan	38,000
Conexant Systems, Incorporated	47,500
Various Donors	15,557
CECS Various Donors	14,515
Sales and Services	17,825
HSSOE Endowed Chair	87,000
Sub Total	\$1,074,305

CONTRACTS, GRANTS AND DONATIONS TOTAL \$5,540,441

DISTINGUISHED LECTURES

“Smart Cameras as High Performance Embedded Systems,” by Professor Wayne Wolf, Princeton University, McDonnell Douglas Auditorium, University of California, Irvine, CA, July 22, 2003

“The Fundamentals: Moore's Law, Microarchitecture, and the Microprocessor of the Year 2014,” by Professor Yale Patt, University of Texas at Austin, McDonnell Douglas Auditorium, University of California, Irvine, CA, December 9, 2003

“System-Level Design: Only the Radical Will Survive,” Dr. Reinaldo Bergamaschi, IBM T.J. Watson Research Center, McDonnell Douglas Auditorium, University of California, Irvine, CA, January 16, 2004

DISTINGUISHED LECTURES (Continue)

“Bluespec: Why chip design can't be left to EE's,” Professor Arvind, CSAIL, Massachusetts Institute of Technology, McDonnell Douglas Auditorium, University of California, Irvine, CA, March 22, 2004

INDUSTRIAL LECTURES

“Embedded Microprocessor Cache and Translation Lookaside Buffer (TLB) Low Power Circuit Techniques for 90nm and Beyond,” by Jonathan R. Haigh and Michael W. Wilkerson, Intel Corporation, McDonnell Douglas Auditorium, University of California, Irvine, CA Industrial Speaker Series, February 6, 2004

COLLOQUIUMS

”Frequent Value Locality and its Applications,” by Rajiv Gupta, University of Arizona, Computer Science Department, McDonnell Douglas Auditorium, University of California, Irvine, CA, May 13, 2004

”Towards Better Compilers & Bug Finding for Sensor Networks,” by Jens Palsberg, UCLA, Computer Science Department, McDonnell Douglas Auditorium, University of California, Irvine, CA, May 24, 2004

“Practical Considerations for Power-Aware Real-Time Scheduling ,” by Sharon Hu, University of Notre Dame, Department of Computer Science and Engineering, McDonnell Douglas Auditorium, University of California, Irvine, CA June 4, 2004

Ph.D. PRESENTATIONS

”Estimation and Exploration Automation of System Level Design,” Lukai Cai presented his final PhD defense at CECS, December 19, 2003

”Specification-driven Validation of Programmable Embedded Systems,” Presented by Prabhat Mishra, University of California, Irvine, March 19, 2004

”System-Level Automatic Model Refinement,” Presented by Junyu Peng, University of California, Irvine, April 2, 2004

“Modeling Flow for Automated System Design and Exploration,” by Andreas Gerstlauer, University of California, Irvine , April 16, 2004

”Communication Synthesis for SoC,” by Dongwan Shin , University of California, Irvine , April 16, 2004

SEMINARS

"Covalidation of Hardware/Software Systems," Presented by Professor Ian G. Harris, University of California, Irvine, Intel Test Research Symposium, Santa Clara, CA, November 7, 2003

"System Debugging and Verification: A New Challenge," Presented by Professor Daniel Gajski and Samar Abdi, University of California, Irvine, Verify 2003, November 20, 2003

"System-Level Design Methodology," Presented by Professor Daniel Gajski, University of California, Irvine, ASP-DAC 2004 , Pacifico Yokohama, Yokohama, Japan, January 27, 2004

SYMPOSIUMS

2003 Southern California Embedded Systems Symposium, September 30, 2003, Beckman Center, Irvine, California

AWARDS

Best Paper Award, October 4, 2003, Dutt, Reshadi, Mishra and Bansal Receive Best Paper Award at CODES+ISSS 2003

SCESS 2003 Award, September 30, 2003, Marshall Lee presenting 2nd place award citation to Sudeep Pasricha, graduate student, UCI

IEEE Computer Society Certificate of Appreciation 2003, A certificate presented for creditable service to any Computer Society activity or program was presented to Professor Ian G. Harris

Prof. Gajski Receives Mentor Award, June 2004, Professor Daniel D. Gajski received the first ever 2004 Graduate Mentor of the Year Award from the Donald Bren School of Information and Computer Sciences. This award was given in recognition of his devotion to graduating 4 Ph.D. students in 2004 and 4 Ph.D. students in 2003

ENEWS LETTERS

eNews: Volume 3, Issue 4 - October 2003 Issue

- 2003 SCESS
- SPARK Tool Release
- Wolf Distinguished Lecture
- Introducing Professors Doemer, Heydari, Scherson
- Configurable Processors
- Publications

ENEWS LETTER (continue)

eNews: Volume 4, Issue 1 - January 2004 Issue

- CECS's Role in International Conference
- Gajski Keynote Address
- Patt Distinguished Lecture
- Arinobu Joins CECS Board
- Gupta EE Times Article
- Inaugurating ICSDS
- Publications

eNews: Volume 4, Issue 2 - April 2004 Issue

- CECS at ASP-DAC
- CECS Goes to DATE
- Arvind Distinguished Lecture
- Bergamaschi Distinguished Lecture
- Haigh-Wilkerson Industrial Speakers
- Gupta Elected IEEE Fellow
- Best Paper Award
- Publications

eNews: Volume 4, Issue 3 - July 2004 Issue

- CECS at DAC
- Introducing Prof. Harris
- Mentor Award to Gajski
- "One Day" FPGA Design Methodology

TOOL RELEASES

SPARK (Release Date: September 19, 2003) Web Site: <http://www.cecs.uci.edu/~spark/>

SPARK is a C-to-VHDL high-level synthesis framework that employs a set of innovative compiler, parallelizing compiler, and synthesis transformations to improve the quality of high-level synthesis results. The compiler transformations have been re-instrumented for synthesis by incorporating ideas of mutual exclusivity of operations, resource sharing and hardware cost models. The SPARK methodology is particularly targeted to control-intensive microprocessor functional blocks and multimedia and image processing applications. We have validated the effectiveness of our approach and evaluated the various optimizations for large real-life applications such as the Instruction Length Decoder from the Intel Pentium and multimedia applications such as MPEG-1, MPEG-2 and the GIMP image processing tool.

Reference: R. Goering, "Tool promises parallelizing synthesis," EE Times, December 19, 2003

BOOKS PUBLISHED

S. Gupta, N. Dutt, R. Gupta, and A. Nicolau. "SPARK: A Parallelizing Approach to the High-Level Synthesis of Digital Circuits," Kluwer Academic Publishers, Norwell, MA, March 2004

JOURNALS**ACM Transactions on Embedded Computing Systems (TECS)**

P. Mishra and N. Dutt, "Automatic Modeling and Validation of Pipeline Specifications," ACM Transactions on Embedded Computing Systems (TECS), Vol 3, No. 1, pp. 114-139, February 2004

P. Mishra, M. Mamidipaka and N.D. Dutt, "Processor-Memory Co-Exploration using an Architecture Description Language," ACM Transactions on Embedded Computing Systems (TECS), Vol 3, No. 1, pp. 140-162, February 2004

IEEE Computers & Digital Techniques

S. Gupta, N. Dutt, R. Gupta, and A. Nicolau, "Dynamically Increasing the Scope of Code Motions During the High-Level Synthesis of Digital Circuits," IEEE (British) Computers & Digital Techniques, Volume 150, Number 5, September 2003, pp 330-337

O. Sinanoglu and A. Orailoglu, "Compacting Test Responses for Deeply Embedded SoC Cores," IEEE Design & Test of Computers, July-August 2003, pp 22-30

IEEE Design & Test of Computers

S. Ozev, I. Bayraktaroglu, and A. Orailoglu, "Seamless Test of Digital Components in Mixed-Signal Paths," IEEE Design & Test of Computers, pp 44-55, January-February 2004

I. G. Harris, "Fault Models and Test Generation for Hardware-Software Covalidation," IEEE Design and Test of Computers, Vol. 20, No. 4, July-August 2003

IEEE Transactions on Circuits and Systems

P. Heydari, "Analysis of the PLL Jitter Due to Power/Ground and Substrate Noise," To appear in IEEE Trans. on Circuits and Systems I, 2004

P. Heydari, S. Abbaspour, and M. Pedram, "Interconnect Energy Dissipation in High-Speed ULSI Circuits," to appear in IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications, 2004

IEEE Transactions on VLSI

P. Heydari and R. Mohanavelu, "Design of Ultra High-Speed Low-Voltage CMOS CML buffers and Latches," to appear in IEEE Trans. on VLSI Systems, 2004

TECHNICAL REPORTS

S. Pasricha and A. Veidenbaum, "Novel Techniques to Improve Branch Prediction Accuracy for Embedded Processors in the Presence of Context Switches," TR 03-24, August 2003

P. Mishra, N. Dutt and H. Tomiyama, "Architecture Description Language driven Validation of Dynamic Behavior in Pipelined Processor Specifications," TR 03-25, July 28, 2003

TECHNICAL REPORTS (continue)

A. Gerstlauer, L.Cai, D. Shin, R. Doemer, and D. Gajski, "System-On-Chip Component Models," TR 03-26, August 11, 2003

N. Bansal, S. Gupta, N. Dutt, A. N, and R. Gupta, "Network Topology Exploration of Mesh-Based Coarse-Grain Reconfigurable Architectures," TR03-27, August 2003

D. Gajski, "NISC: The Ultimate Reconfigurable Component," TR 03-28, October 1, 2003.

S. Abdi and D. Gajski, "Provably Correct Architecture Refinement," TR 03-29, September 30, 2003

A. Gerstlauer, "Communication Abstractions for System-Level Design and Synthesis," TR 03-30, October 24, 2003

S. Abdi and D. Gajski, "System Debugging and Verification: A New Challenge," TR 03-31, October 1, 2003

M. Mamidipaka, K. Khouri, N. Dutt, and M. Abadir, "Leakage Power Estimation in SRAMs," TR 03-32, October 24, 2003

D. Shin, S. Abdi, and D. Gajski, "Automatic Generation of Bus Functional Models from Transaction Level Models," TR 03-33, November 18, 2003

A. Nacul and T. Givargis, "Dynamic Voltage and Cache Reconfiguration for Low Power," TR 03-34, November 7, 2003

R. Jejurikar, C. Pereira, and R. Gupta, "Leakage Aware Dynamic Voltage Scaling for Real Time Embedded Systems," TR 03-35, November 30, 2003

A. Nacul, S. Choudhuri, and T. Givargis, "POSIX-Compliant Portable Code Synthesis for Embedded Systems," TR 03-36, November 25, 2003

A. Kejariwal, S. Gupta, A. Nicolau, N. Dutt, and R. Gupta, "Energy Analysis of Multimedia Watermarking on Mobile Handheld Devices," TR 03-38, November 2003

N. Savoiu, S. Shukla, and R. Gupta, "Petri Net-based Thread Composition for Improved System Level Simulation," TR 03-39, December 29, 2003

S. Banerjee and N. Dutt, "FIFO Power Optimization for On-Chip Networks," TR 03-40, December 19, 2003

S. Abdi, J. Peng, H. Yu, D. Shin, A. Gerstlauer, R. Doemer, and D. Gajski, "System-on-Chip Environment: SCE Version 2.2.0 Beta Tutorial," TR 03-41, December 2003

D. Shin, A. Gerstlauer, R. Doemer, and D. Gajski, "C-based Interactive RTL Design Methodology," TR 03-42, December 1, 2003

R. Jejurikar and R. Gupta, "Energy Aware Non-preemptive Scheduling for Hard Real-Time Systems," TR 04-01, January 21, 2004

TECHNICAL REPORTS (continue)

TR 04-02 (pending release due to conference proceeding submission)

R. Jejurikar and R. Gupta, "Integrating Processor Slowdown and Preemption Threshold Scheduling for Energy Efficiency in Real Time Embedded Systems," TR 04-03, February 16, 2004

L. Cai, A. Gerstlauer, and D. Gajski, "Retargetable Profiling for Rapid, Early System-Level Design Space Exploration," TR 04-04, October 2003

P. Mishra and N. Dutt, "Functional Coverage Driven Test Generation for Validation of Pipelined Processors," TR 04-05, March 12, 2004

S. Pasricha, M. Ben-Romdhane, and N. Dutt, "High Level Design Space Exploration of Shared Bus Communication Architectures," TR 04-06, March 13, 2004

N. Savoiu, S. Shukla, and R. Gupta, "A Semantics-Preserving Reduction of Code-Annotated Well-formed Free Choice Petri Nets," TR 04-07, February 12, 2004

M. Reshadi and D. Gajski, "NISC Modeling and Simulation," TR 04-08, March 2004

R. Jejurikar and R. Gupta, "Procrastination Scheduling in Fixed Priority Real-Time Systems," TR 04-09, April, 2004

R. Jejurikar and R. Gupta, "Optimized Slowdown in Real-Time Task Systems," TR 04-10, April 2004

S. Pasricha, N. Dutt, and M. Ben-Romdhane, "Rapid Exploration of Bus-based Communication Architectures at the CCATB Abstraction," TR 04-11, May 2004

M. Reshadi and D. Gajski, "NISC Application and Advantages," TR 04-12, May 2004

I. G. Harris, "On the Detection of Synchronization Errors," TR 04-13, May 2004

R. Jejurikar and R. Gupta, "Systemwide Energy Minimization in Real-Time Embedded Systems," TR 04-14, May 2004

D. Shin, A. Gerstlauer, and D. Gajski, "Network Synthesis for SoC," TR 04-15, June 10, 2004

D. Shin, A. Gerstlauer, and D. Gajski, "Communication Link Synthesis for SoC," TR 04-16, June 10, 2004

P. Chandraiah, H. Schirner, N. Srinivas, and R. Doemer, "System-On Chip Modeling and Design: A Case Study on MP3 Decoder," TR 04-17, June 21, 2004

CONFERENCE PROCEEDINGS

IEEE High-Level Design, Validation, and Test Workshop (HLDVT 2003)

E. Gaudette, M. Moussa, and I. G. Harris, "A Method for the Evaluation of Behavioral Fault Models,"

CONFERENCE PROCEEDINGS (continue)

IEEE High-Level Design, Validation, and Test Workshop (HLDVT), November 2003

First Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia 2003)

S. Pasricha, S. Mohapatra, M. Luthra, N. Dutt, and N. Venkatasubramanian, "Reducing Backlight Power Consumption for Streaming Video Applications on Mobile Handheld Devices," ESTIMedia 2003, First Workshop on Embedded Systems for Real-Time Multimedia, Newport Beach, CA, October 2003

International Conference on Computer Design (ICCD 2003)

S. Pasricha, and A. Veidenbaum, "Improving Branch Prediction Accuracy in Embedded Processors in the Presence of Context Switches," International Conference on Computer Design (ICCD 2003), San Jose, CA, October 2003

CODES + ISSS 2003

L. Cai and D. Gajski, "A Transaction Level Modeling: An Overview," First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, pp 19-24, Newport Beach, CA, October 2003

S. Cotterell, F. Vahid, W. Najjar and H. Hsieh, "First Results with eBlocks: Embedded Systems Building Blocks," First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, pp 168-175, Newport Beach, CA, October 2003

A. Koohi, N. Bagherzadeh, and C. Pan, "A Fast Parallel Reed-Solomon Decoder on a Reconfigurable Architecture," First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, pp 59-64, Newport Beach, CA, October 2003

B. Mohebbi, E. Filho, R. Maestre, M. Davies, and F. Kurdahi, "A Case Study of Mapping a Software Defined Radio (SDR) Application on a Reconfigurable DSP Core," First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, pp 103-108, Newport Beach, CA, October 2003

M. Reshadi, N. Bansa, P. Mishra and N. Dutt, "An Efficient Retargetable Framework for Instruction-Set Simulation," First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, pp 13-18, Newport Beach, CA, October 2003

H. Yu, A. Gerstlauer, and D. Gajski, "RTOS Scheduling in Transaction Level Models," First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, pp 31-36, Newport Beach, CA, October 2003

IEEE International Test Conference 2003

D. A. Fernandes and I. G. Harris, "Application of Built in Self-Test for Interconnect Testing of FPGAs," IEEE International Test Conference, September 2003

CONFERENCE PROCEEDINGS (continue)**2003 International Symposium on Low Power Electronics and Design (ISLPED 2003)**

P. Chou, C. Park, J. Park, K. Pham, and J. Liu, "B#: a Battery Emulator and Power Profiling Instrument," 2003 International Symposium on Low Power Electronics and Design, pp 288-293, Seoul, Korea, August 2003

P. Heydari and Y. Zhang, "A Novel High Frequency, High-Efficiency, Differential Class-E Power Amplifier in 0.18 μ m CMOS, Payam Heydari, and Ying Zhang," 2003 International Symposium on Low Power Electronics and Design, pp 455-458, Seoul, Korea, August 2003

J. Lee, K. Choi, and N. Dutt, "Energy-Efficient Instruction Set Synthesis for Application-Specific Processors," 2003 International Symposium on Low Power Electronics and Design, pp 330-333, Seoul, Korea, August 2003

D. Nicolaescu, A. Veidenbaum, and A. Nicolau, "Reducing Data Cache Energy Consumption via Cached Load/Store Queue," 2003 International Symposium on Low Power Electronics and Design, pp 252-257, Seoul, Korea, August 2003

Design Automation Conference 2004 (DAC 2004)

S. Abdi and D. Gajski, "Automatic Generation of Equivalent Architecture Model from Functional Specification," Design and Automation Conference (DAC 2004), pp 608-613, June 7-11, 2004

P. Biswas, V. Choudhary, K. Atasu, L. Pozzi, P. Ienne, and N. Dutt, "Introduction of Local Memory Elements in Instruction Set Extensions," Design and Automation Conference (DAC 2004), pp 729-734, June 7-11, 2004

L. Cai, A. Gerstlauer, and D. Gajski, "Retargetable Profiling for Rapid, Early System-Level Design Space Exploration," Design and Automation Conference (DAC 2004), pp 281-286, June 7-11, 2004

R. Jejurikar, C. Pereira, and R. Gupta, "Leakage Aware Dynamic Voltage Scaling for Real-Time Embedded Systems," Design and Automation Conference (DAC 2004), pp 275-280, June 7-11, 2004

A. Kejariwal, S. Gupta, A. Nicolau, N. Dutt and R. Gupta, "Proxy-Based Task Partitioning of Watermarking Algorithms for Reducing Energy Consumption in Mobile Devices," Design and Automation Conference (DAC 2004), pp 556-561, June 7-11, 2004

R. Lysecky, F. Vahid, and S. Tan, "Dynamic FPGA Routing for Just-in-Time FPGA Compilation," Design and Automation Conference (DAC 2004), pp 659-662, June 7-11, 2004

S. Pasricha, N. Dutt, M. Ben-Romdhane, "Extending the Transaction Level Modeling Approach for Fast Communication Architecture Exploration," Design and Automation Conference (DAC 2004), pp 113-118, June 7-11, 2004

IEEE International Symposium on Circuits and Systems (ISCAS 2004)

A. Yazdi and P. Heydari, "A Novel Non-Uniform Distributed Amplifier," to appear in IEEE International Symposium on Circuits and Systems, May 23-26, 2004

CONFERENCE PROCEEDINGS (continue)

A. Safarian and P. Heydari, "Design and Analysis of a Distributed Regenerative Frequency Divider Using a Distributed Mixer," to appear in IEEE International Symposium on Circuits and Systems, May 23-26, 2004

Ravindran Mohanavelu and Payam Heydari, "A Novel Ultra High-Speed Flip-Flop-Based Frequency Divider," to appear in IEEE International Symposium on Circuits and Systems, May 23-26, 2004

Asia South Pacific Design Automation Conference 2004 Pacifico Yokohama (ASP-DAC 2004)

S. Abdi and D. Gajski, "On Deriving Equivalent Architecture Model from System Specification," Asia and South Pacific Design Automation Conference (ASP-DAC 2004), Yokohama, Japan, pp 322-327, January 27-30, 2004

L. Cai, H. Yu and D. Gajski, "A Novel Memory Size Model for Variable-Mapping in System Level Design," Asia and South Pacific Design Automation Conference (ASP-DAC 2004), Yokohama, Japan, pp 813-818, January 27-30, 2004

B. Gorji-Ara, P. Chou, N. Bagherzadeh, M. Reshadi and D. Jensen, "Fast and Efficient Voltage Scheduling by Evolutionary Slack Distribution," Asia and South Pacific Design Automation Conference (ASP-DAC 2004), Yokohama, Japan, pp 659-662, January 27-30, 2004

P. Heydari, "High-Frequency Noise in RF Active CMOS Mixers," Asia and South Pacific Design Automation Conference (ASP-DAC 2004), Yokohama, Japan, pp 57-61, January 27-30, 2004

SLIDE PRESENTATIONS**5th International Conference on ASIC (ASICON 2003)**

D. Gajski, "SoC Design for the New Millennium," 5th International Conference on ASIC (ASICON 2003), Beijing, China, October 21, 2003.

First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2003)

D. Gajski and L. Cai, "Transaction Level Modeling," First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2003), Newport Beach, CA, October 1, 2003.

Design Automation Conference 2004 (DAC 2004)

D. Gajski, "Good Old Days: EDA Then and Now," DAC 2004, San Diego, CA, June 9, 2004

Asia South Pacific Design Automation Conference 2004 Pacifico Yokohama (ASP-DAC 2004)

D. Gajski, "System-Level Design Methodology," ASP-DAC 2004 Pacifico Yokohama, Yokohama, Japan, January 27, 2004

SLIDE PRESENTATIONS (continue)

A. Shrivastava and N. Dutt, "Energy Efficient Code Generation Using rISA," ASP-DAC 2004 Pacifico
Yokohama, Yokohama, Japan, January 27, 2004

H. Yu, R. Doemer, and D. Gajski, "Embedded Software Generation from System Level Design
Languages," ASP-DAC 2004 Pacifico Yokohama, Yokohama, Japan, January 27, 2004