

Ph.D. Defense Announcement

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Analysis and Optimization of Transaction Level Models for Multi-Processor System-on-Chip Design

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Embedded Systems are omnipresent in our environment for example as digital media devices, mobile phones, or control systems. Their increase in complexity poses great challenges to the design process, and an exploding number of architecture alternatives have to be evaluated to derive an efficient implementation. Additionally, today's embedded systems become more software centric, and software development clearly dominates the design cost. System-Level Design addresses these challenges by using a unified approach for hardware and software design. Raising the level of abstraction, system-level design uses abstract HW/SW models, Transaction Level Models (TLM), for system analysis, exploration, simulation, and synthesis. Well-defined and efficient models are crucial for a reliable design space exploration. In particular, fast yet accurate models are needed to improve the end product and reduce the design time.

We contribute in three aspects. First, we systematically analyze communication models and quantify the speed/accuracy trade-off in TLM. Each abstraction level improves the simulation speed by several orders of magnitude, however at a significant loss of accuracy. Second, we propose a novel technique, Result Oriented Modeling (ROM), which removes the inaccuracy drawback of TLM, yet yields nearly the same speed. Third, we propose a fast alternative to traditional instruction set simulation that shows speed gains of three orders of magnitude with only a few percent error in timing accuracy. Overall, our work guides the system developer in choosing proper model features and provides efficient techniques to model them. It supports the designer in model selection, analysis and implementation. As a result, our system modeling research will influence the design of digital embedded systems, resulting in better and less expensive end products while reducing the time-to-market.