

DISTINGUISHED LECTURE

Center for Embedded Computer Systems

Presents

Hardware-Accelerated Formal Verification

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Abstract

A semi-formal verification technique, which performs a brute-force compiled simulation with a sophisticated search space pruning, has been proposed and shown to be competitive with the state-of-the-art SAT-based verification techniques, especially for complicated logics such as hardware having various arithmetic computation units. We have enhanced this technique by using an FPGA-based hardware accelerator (a kind of FPGA emulation but targeting formal verification), and our preliminary results showed that our verifier is about 7 times faster than the original software-based semi-formal verifier running on the state-of-the-art processors. The approach is a sort of hardware/software co-design and co-execution approach to formal verification. We demonstrate our techniques on PC with extra FPGA board implementation.

Biography

Masahiro Fujita received his Ph.D. from the University of Tokyo in 1985. He is a professor in VLSI Design and Education Center (VDEC) at the University of Tokyo. Prior to joining the University of Tokyo in 2000, he was director of CAD for VLSI in Fujitsu Laboratories of America for 6 years. He has done innovative works in the areas of digital design verification, synthesis, and testing. He has co-authored 7 books, and has over 150 publications. He has been given several research awards from Japanese scientific societies. His current research interests include synthesis and verification in higher level design stages, hardware/software co-designs and also digital/analog co-designs.

Tuesday, April 29th, 2008

Refreshments at 2:30pm, Lecture begins at 3:00pm

McDonnell Douglas Auditorium

Host: Professor Daniel Gajski

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