

COLLOQUIUM

Center for Embedded Computer Systems

Presents

High level systems validation using hierarchical message sequence charts

Dr. Praveen Murthy
Fujitsu Labs of America

Abstract

As electronic systems become more complex, a greater percentage of time is being spent in validating designs. One way of solving this issue is by raising the level of abstraction at which designs are specified. At Fujitsu, there is great interest in using UML and UML-like languages for specifying designs, even those that will be implemented purely in hardware. Dr. Murthy will discuss ongoing work at Fujitsu labs where the researchers have been using hierarchical message sequence charts (a more expressive model of computation that subsumes many UML 2.0 behavioral diagrams such as sequence, interaction, and state charts) to specify reactive protocols and generating test suites automatically. These techniques have been applied on an actual PCI-Express physical layer design and found effective.

Biography

Praveen Murthy has been at Fujitsu labs of America (FLA) since 2001. He is interested in all aspects of system level design and leads the Scenery project at FLA. Before joining FLA, he was with the startup Angeles design systems, where he was one of the architects of System Canvas, and before that at Cadence design systems where he developed dataflow compiler optimization algorithms. He holds a Ph.D. in EECS from UC Berkeley, and B.S. in EE from Georgia Tech.

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Calit2 Auditorium

Talk begins at 2:30pm; Refreshments at 2:00pm

CECS Host: Nikil Dutt, dutt@ics.uci.edu

For more information contact: Melanie Kilian at (949) 824-9127